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DFE-T V2.2

Quad ISDN 4B3T Echocanceller Digital Front End
PEF 24901, Version 2.2

Wired Communications

Infineon technologies

Never stop thinking.

Data Sheet

Revision History:	**2002-09-30**	DS1
Previous Version:	Preliminary Data Sheet, DS1, 6.99	

Page	**Subjects (major changes since last revision)**
	update related documents
Chapter 1	conforms to ITU-T G.961 (not ITU-T I.430) removed transparent channel
Chapter 1.1	Removed: Sophisticated power management for restricted power mode Removed: Monitor Time-Out (MTO) procedure 'LTD' supported Coefficients are no more retrievable by MON-8 commands
Figure 2, **Figure 6**, **Table 1**	logic symbol, pin conf., pin definitions: removed TP1, MTO 49, 53: no function, may be clamped to GND or VDD, respectively, for compatibility to former versions
Chapter 1.3	added DELIC-PB, restriction on DELIC-PB, added Vbat, removed solution with ELIC/IDEC (IDEC is discontinued)
Page 19	added note on CLOCK and FSC from same source
Figure 4	added connection between pin CLOCK and FSC
Table 1, **Table 2**	changed: pins CLS 0..3 indicate 1 ms clock of the received frame.
Table 1	added footnote to PU/PD to TCK in case that JTAG is reset: e.g. pull-down 47 kΩ
Table 1	removed from all PD/PU-pins: internal pullup (160 kΩ), added footnote to PU/PD: e.g. 10 to 20 kΩ
Table 1	removed from PUP: (as soon as 1.FSC was received after reset)
Chapter 2.3	updated pinning changes
Table 3	added new table 'pin controlled test modes'
Chapter 3.1	removed dedicated block diagram
Chapter 3.2.2	replaced double last look criterion by real reaction times
Chapter 3.2.3	removed MON0 commands
Chapter 3.2.3	removed MTO function
Chapter 3.3	$\overline{\text{NOP}}$ is always set to one added note: activation of the interface to the analog front end

Data Sheet

Revision History: **2002-09-30**   DS1

Chapter 3.5	removed from 1 kHz Frame: '..40 kHz block clock'
Chapter 3.5.1	removed 'After successful synchronization, resynchronization will occur if the syncword is not detected at the expected position in 64 consecutive frames. The U-transceiver is synchronized, if it detects the syncword four times consecutively within a period of 1 ms.'
Chapter 3.5.8, Chapter 3.5.11.2	removed U2A (not supported)
Page 15, Page 45	removed statement on performance on 0.6mm FTZ loops
Page 47	removed transparent messages
Table 12	refined description of signal detection, removed transparent channel from table 4B3T signal elements
Chapter 3.5.9	refined description C/I-codes, changed validation times of C/I-commands, introduced LTD
Figure 17	updated state machine
Table 14	updated differences to the former state machine
Chapter 3.5.11.1	changes to state machine inputs: C/I=AR1: no reset of receiver C/I DC: state Deactivted is entered
Chapter 3.5.11.2	C/I-indication 'AI' is also issued if test loop #1 has been activated
Page 64	Transparent state may also be entered by loopback 1 (not loopback 2)
Chapter 3.5.5	reworked chapter block error counter
Chapter 3.5.11.1	AR1, AR2, and AR4: added description of resolving loopback requests
Chapter 3.6	changed chapter 'clock generation',
Chapter 4.1	added to HW reset: '...the 15.36 MHz ...', ' ...Note that FSC and DCL...'
Chapter 4.2	the DFE-T goes in power down, if the U-transceiver is in state 'Deactivated' and no MONITOR message is pending
Figure 26	testloops repeater: #4
Chapter 4.4.1.2	removed fig: 'Loopback #2'

Data Sheet

Revision History: **2002-09-30**   DS1

Figure 27	reworked
Chapter 4.4.1.3	DLB is always transparent
Chapter 4.4.2	reworked chapter RDS, added note with active states
Chapter 4.4.3	reworked operation
Chapter 4.4.4.2	added note: Data Through is pure test mode
Chapter 4.4.5	removed chapter: DSP access - not supported
Chapter 4.4.5	added note on pin 16 and 49
Table 18	changed coding of instruction BYPASS: '1111' (instead of '11XX')
Table 19 **Table 20**	restricted tables to commands and indications for DFE-T V2.2
Table 19	added note on response to 87xxh
Table 20	coding of MON-8 command AST = '810X' (not '880X'); AST is sent in upstream direction
Page 89	removed MON-0: not supported
Chapter 6	reworked fig. DFE-T V2.2 Register Map
Chapter 6.1	reworked register summary
Chapter 6.1.1 **Chapter 6.1.2**	new chapters added: registers TEST and LOOP are evaluated and executed immediately
Chapter 6.2	reworked detailed register description
Chapter 7.1	updated
Chapter 7.2	updated
Chapter 7.3	updated
Figure 29	removed 100 pF load capacitance
Chapter 7.4	updated
Table 23 **Table 25**	updated
Chapter 7.5	removed clock input capacitance
Chapter 7.6	updated

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Preface

This document describes the interfaces, functions and behavior of the QUAD ISDN 4B3T Echocanceller Digital Front End (DFE-T V2.2). The PEF 24901 is the digital part of a two-chip solution featuring four times ISDN basic rate access at 144 kbit/s. DFE-T V2.2 supersedes the existing versions, DFE-T V1.1 and DFE-T V1.2.

The corresponding Analog Front End, the AFE V2.1 (PEF 24902) is described in detail in the Data Sheet V1.1, the Delta Sheet V1.2 and the Data Sheet V2.1.

Organization of this Document

This Data Sheet is divided into 9 chapters. It is organized as follows:

- **Chapter 1**, Introduction
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- **Chapter 2**, Pin Description
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3**, Functional Description
  Gives a functional overview of the device, shows a block diagram, specifies the various interfaces and describes the provided U-transceiver functions.

- **Chapter 4**, Operational Description
  Describes the reset and power-down behavior, illustrates the activation and deactivation procedures, shows how the device is tested and how maintenance data can be retrieved.

- **Chapter 5**, Monitor Commands
  Lists all available Monitor Commands that can be applied.

- **Chapter 6**, Register Description
  Lists all register functions that are addressable by the new MON-12 protocol.

- **Chapter 7**, Electrical Characteristics
  Denotes the operating conditions and gives the exact interface timing.

- **Chapter 8**, Package Outlines

- **Chapter 9**, Appendix A: Standards and Specifications

- **Chapter 10**, Terminology

- **Chapter 11**, Index

Related Documentation

- DFE-T V2.2 Product Brief 03.01
- DFE-T V2.2 Delta Sheet 11.01
- AFE V1.1 Data Sheet 05.96
- AFE V1.2 Delta Sheet 06.97
- AFE V2.1 Data Sheet 01.01

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1 Introduction

The Quad ISDN 4B3T Echocanceller Digital Front End (DFE-T) is the digital part of an optimized two-chip solution featuring 4x ISDN basic rate access at 144 kbit/s. The PEF 24901 is designed to provide in conjunction with the Quad ISDN Echocanceller Analog Front End (PEF 24902 V2.1) full duplex data transmission at the U-reference point according to FTZ Guideline 1TR 220, ETSI TS 102 080 and ITU-T G.961 standards.

The DFE-T 2nd generation has been completely reengineered to guarantee the availability of the well proved DFE-T/AFE solution over the year 2000. PEF 24901 V2.2 is downwards pin compatible and functionally equivalent to the DFE-T V1.x. Thus, line card manufacturers can make use of the most advanced process technology without the need to change their current design (besides the changeover to 3.3 V power supply).

No software changes are required if the DFE-T V2.2 is deployed in existing DFE-T V1.x solutions. Some new features are provided such as enhanced monitoring and test functions. The data rate is programmable from 1 Mbit/s to 4 Mbit/s.
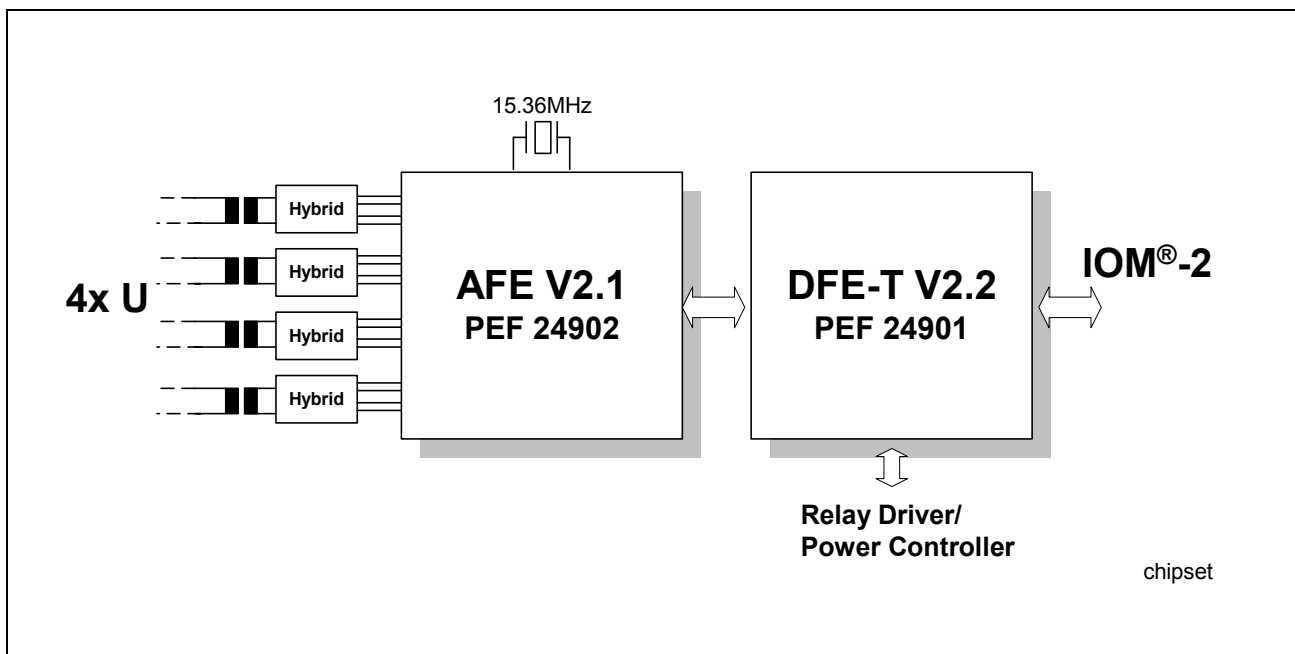
Figure 1   DFE-T/ AFE 2nd Generation Chip Set

The output and input pins are throughout 5 V TTL compatible although the PEF 24901 is processed in advanced 3.3 V CMOS technology. A power down state with very low power consumption is featured.

The PEF 24901 comes in a P-MQFP-64 package.

Quad ISDN 4B3T Echocanceller Digital Front End   **PEF 24901**
DFE-T V2.2

Version 2.2

1.1 Features

U-Interface

P-MQFP-64-1, -2, -3, -8

- Digital part of a two-chip solution featuring full duplex data transmission and reception over two-wire metallic subscriber loops providing 4x ISDN basic rate access at 144 kbit/s
- Conforms to:
  - FTZ 1TR 220 (1991)
  - ETSI TS 102 080 V1.3.1 (1998)
  - ITU-T G.961 (1995)
- 4B3T-block code at 120-kHz symbol rate
- Subscriber loop length without repeater:
  - up to 4.2 km on 0.4 mm wire
- LT mode
- 1 kbit/s maintenance channel for transmission of data loopback commands and detected transmission errors
- Activation/ deactivation controller
- Adaptive echo cancellation and equalization
- Automatic gain control and polarity adaption
- Clock recovery (frame and bit synchronization)
- Transmission error counters for line monitoring
- Remote and local control of test loops
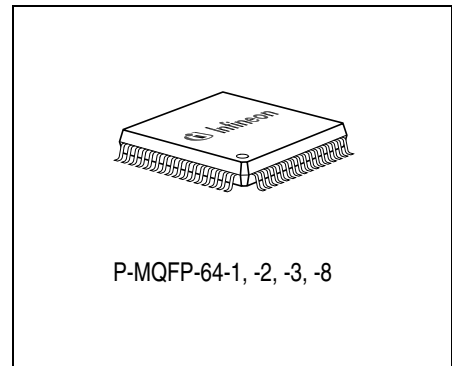
System Interface

- IOM$^®$-2 interface with programmable data rates (1 Mbit/s to 4 Mbit/s)
- 4 relay driver pins per port addressable by Monitor command
- 2 status pins per port accessible via Monitor channel

Type	Package
PEF 24901	P-MQFP-64

Other Features

- Software compatible to the PEF 24901 V1.2
- Inputs and outputs 5 V TTL compatible
- DOUT (open drain) accepts pull-up to 3.3 V or 5 V
- Advanced low power CMOS technology
- +3.3 V ±0.3 V Power Supply
- Extended temperature range (– 40 ... to 85 °C) available
- Boundary-Scan, JTAG IEEE 1149.1

Add-On Features and Differences with Respect to DFE-T V1.2

- +3.3 V instead of +5 V power supply
- LT-RP mode is not supported
- DOUT configurable either as open drain or push-pull (tristate) output
- Bit Error Rate measurement per port
- Additional digital local loops
- C/I code 'HI' are no more supported
- C/I code mnemonics adapted to 2B1Q notation for consistency reasons - coding has been retained unchanged
- State machine notation is aligned to that of 2B1Q for consistency reasons
- New MON-12 class features internal register access
- Coefficients are no more retrievable by MON-8 commands
- The Boundary-Scan instructions 'CLAMP' and HIGHZ are supported in version 2.2 ('SSP' is omitted since for this function a dedicated pin is reserved)
- JTAG Boundary-Scan with dedicated reset line $\overline{\text{TRST}}$ (replaces power-on reset functionality)

1.2 Logic Symbol
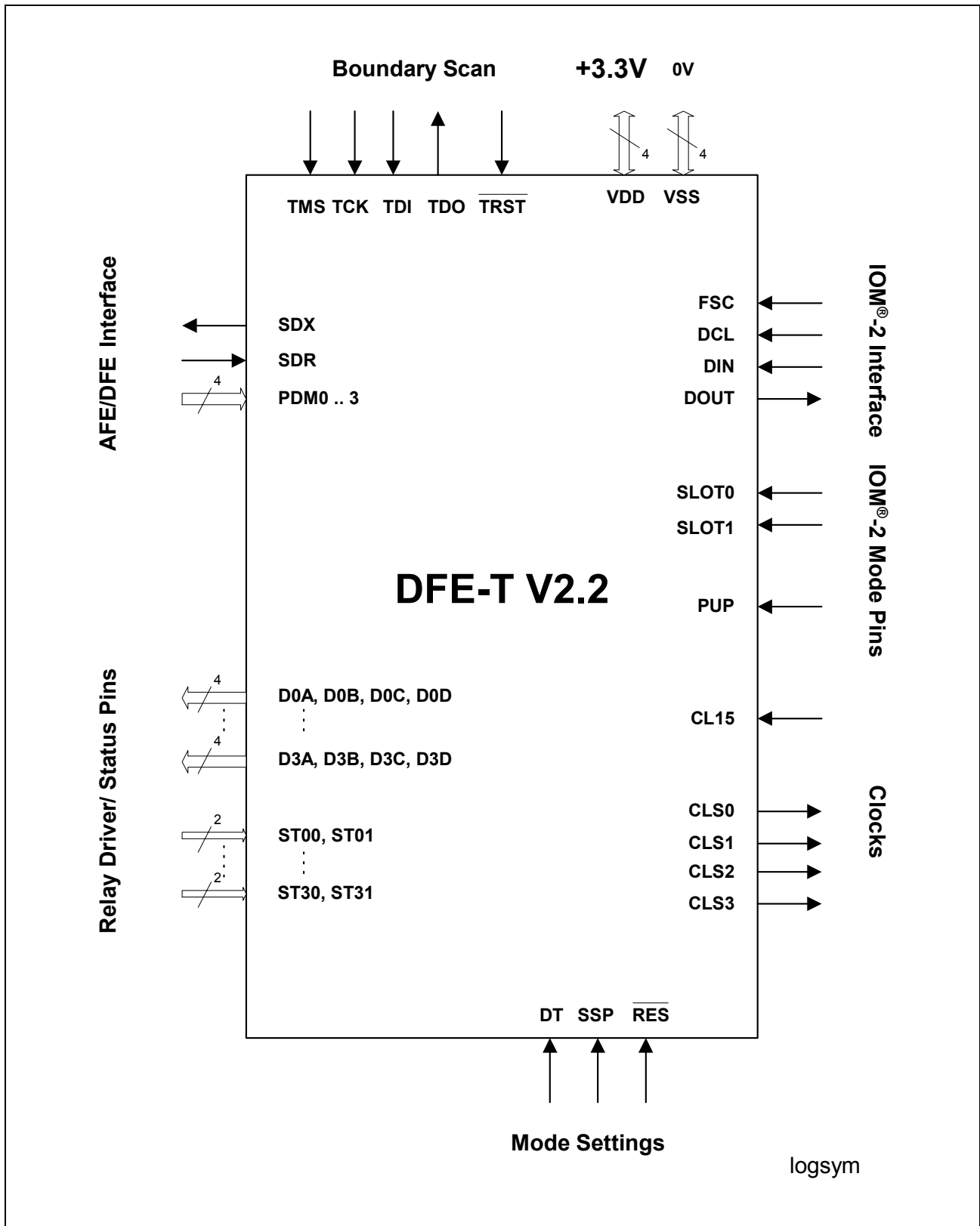
Figure 2 Logic Symbol

1.3 System Integration

This paragraph shows how the DFE-T V2.2 may be integrated in systems using other Infineon ISDN devices. The PEF 24901 V2.2 is optimized for use in the following applications:

– Digital Line Cards for Central Office
– Digital Line Cards for Access Networks (LT mode only)
– PBX applications (LT mode only)

Figure 3 illustrates a line card solution. The DELIC-PB (PEB 20571) supersedes the ELIC® (PEB 20550) and features up to 32 HDLC controllers on-chip. The DELIC controls up to 4 devices of DFE-T V2.2 on a single IOM®-2 interface. In this application an additional clock doubler is necessary to generate the 8.192 MHz DCL clock for the DFE-T derived from the 4.096 MHz BCL clock of the DELIC.
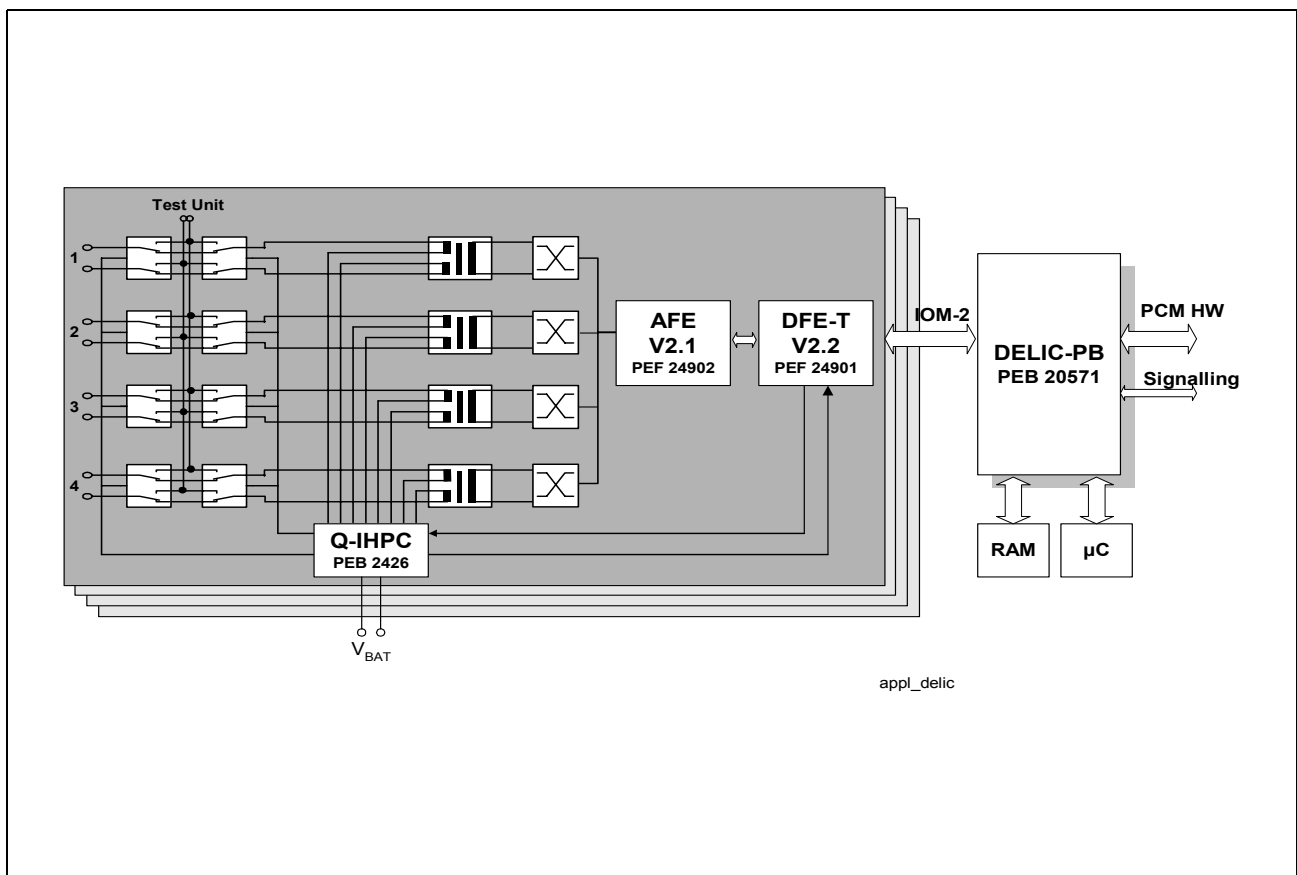
Figure 3   16-Line Card Application with DELIC-PB Solution

Figure 4 shows how a 8 channel line card application is realized by use of two AFE/ DFE-T chip sets:

One AFE PLL generates the synchronized 15.36 MHz clock and provides the master clock at pin CL15 for the other 3 devices. The internal PLL of the first AFE synchronizes the 15.36 MHz master clock onto a PTT reference clock of either 8 kHz or 2048 kHz. **Infineon recommends to feed the FSC clock input of the DFE-T V2.2 and the PLL reference clock input (pin CLOCK) of the AFE from the same clock source.**

The PLL of the second AFE is deactivated. The 15.36 MHz master clock is applied at pin CL15. CL15 is configured as input if XIN is clamped either to VDD or to VSS. Pin XOUT has to be left open and CLOCK shall be tied to GND.
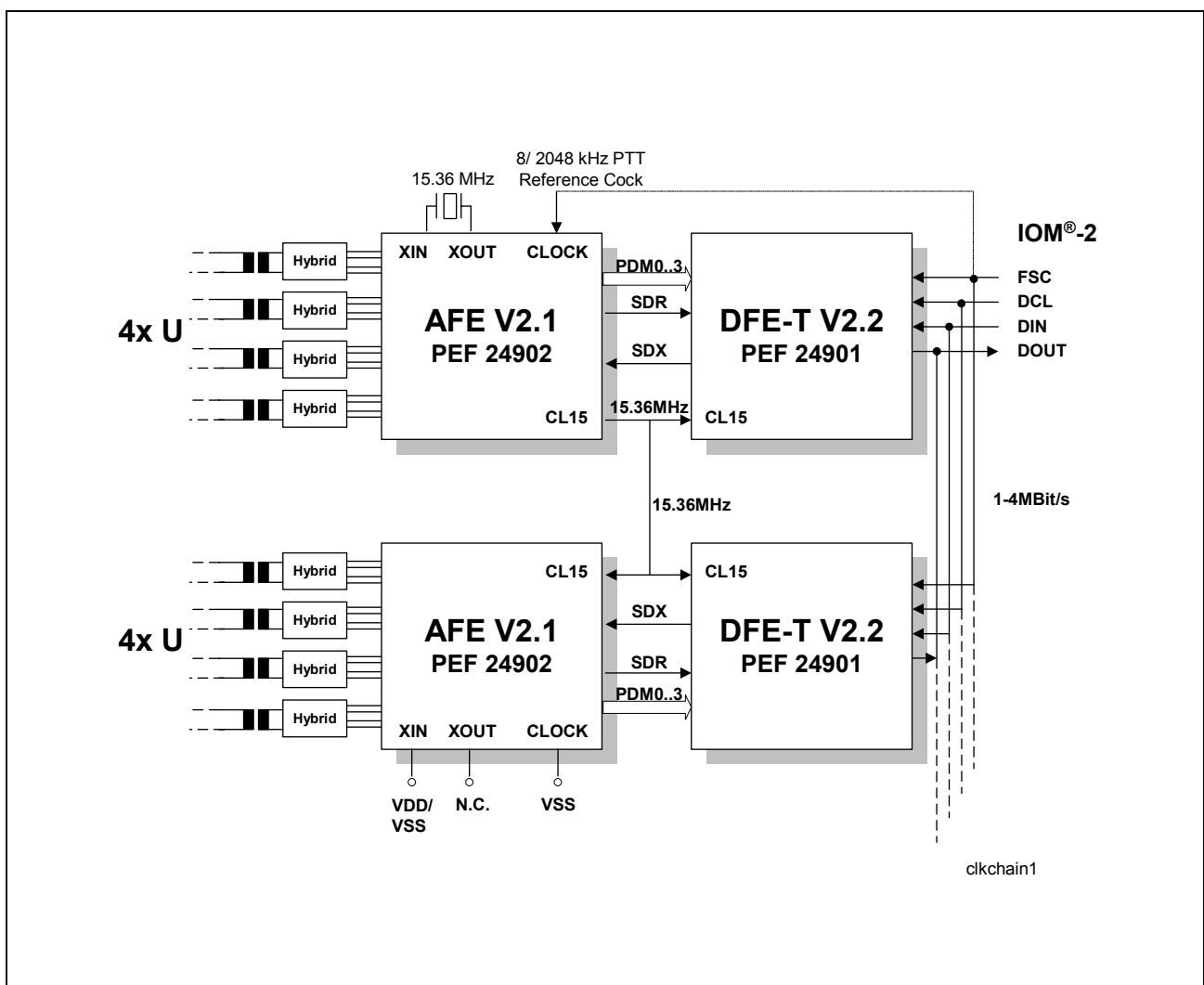
Figure 4   Connecting Two AFE/DFE-T Chip Sets

The DFE-T devices are supplied by the first AFE at pin CL15 with the synchronized 15.36 MHz clock. The IOM®-2 channels the DFE-T devices are assigned to can be programmed by the two slot pins. Starting from channel no. 0/4/8/12 always four subsequent channels are occupied.

Alternatively the clocking scheme as shown in **Figure 5** may be applied if more than 3 devices are to be clocked (e.g. in a 16-channel line card application). Instead to supply the 2nd AFE with the master clock at pin CL15, here the 15.36 MHz master clock is input at pin XIN. Thereby pin CL15 is configured as output and passes the 15.36 MHz clock on to the attached DFE-T. If the clock chain is extended in the same way by another two AFE/DFE-T chip sets a 16-channel line card application can be realized with just one single crystal. Note that the 15.36 MHz clock is inverted once by the AFE if it is input at XIN and output at CL15. This way the duty cycle is recovered again.
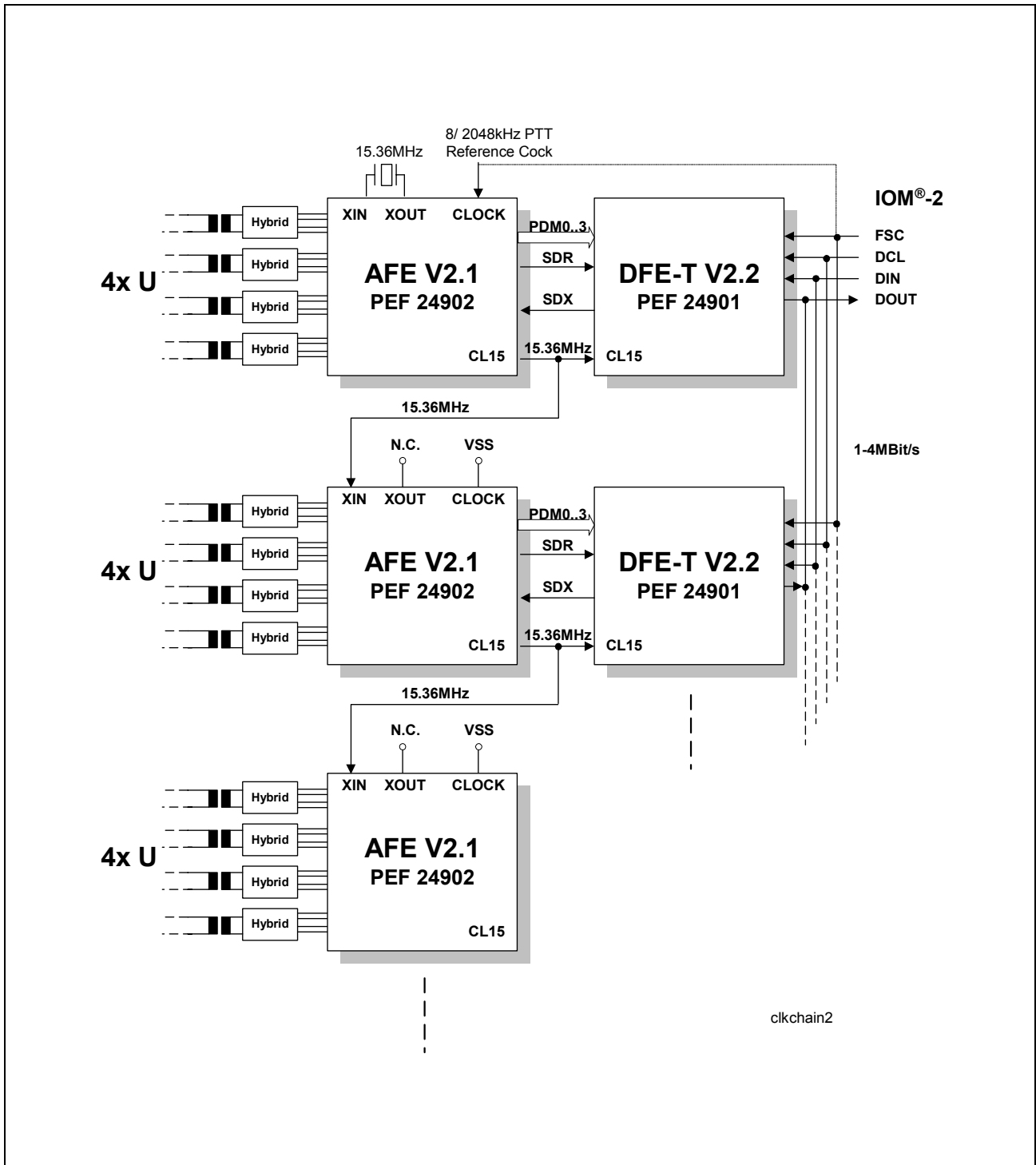
Figure 5   Recommended Clocking Scheme for More Than Two DFE-T/AFE Chip Sets

1.4   Operational Overview

The DFE-T V2.2 operates always in LT mode.

System Interface Configurations

The following parameters of the system interface are configurable:

- Open Drain/ Push-Pull Mode
  Configured as open drain the output pin DOUT is floating and a pull-up resistor is required. In push-pull mode the output pin is high impedance outside the active time slots.
- IOM$^{®}$-2 Channel Assignment
  IOM$^{®}$-2 channels are always assigned in blocks of four.

SLOT1	SLOT0	Assigned IOM$^{®}$-2 Channels
0	0	0 .. 3
0	1	4 .. 7
1	0	8 .. 11
1	1	12 .. 15

- IOM$^{®}$-2 Data Rates

DCL Frequency [kHz]	Data Rate [kBit/s]	IOM$^{®}$-2 Channels
2048	1024	4
3072	1536	6
4096	2048	8
6144	3072	12
8192	4096	16

Send Single Pulses Test Mode

In test mode 'Send Single Pulses' +1 pulses spaced by 1 ms are transmitted on all U lines. The test mode is activated by pin SSP= set to '1'. The SSP test function can be as well stimulated by C/I= SSP besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line.

Data Through Mode

In test mode 'Data Through' the U-transceiver is forced to enter the 'Transparent' state and to issue U4 independently of the wake-up protocol. The DT test mode is activated by pin DT= set to '1'. The DT test function can be as well stimulated by C/I= DT besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line.

2 Pin Descriptions

2.1 Pin Diagram

(top view)
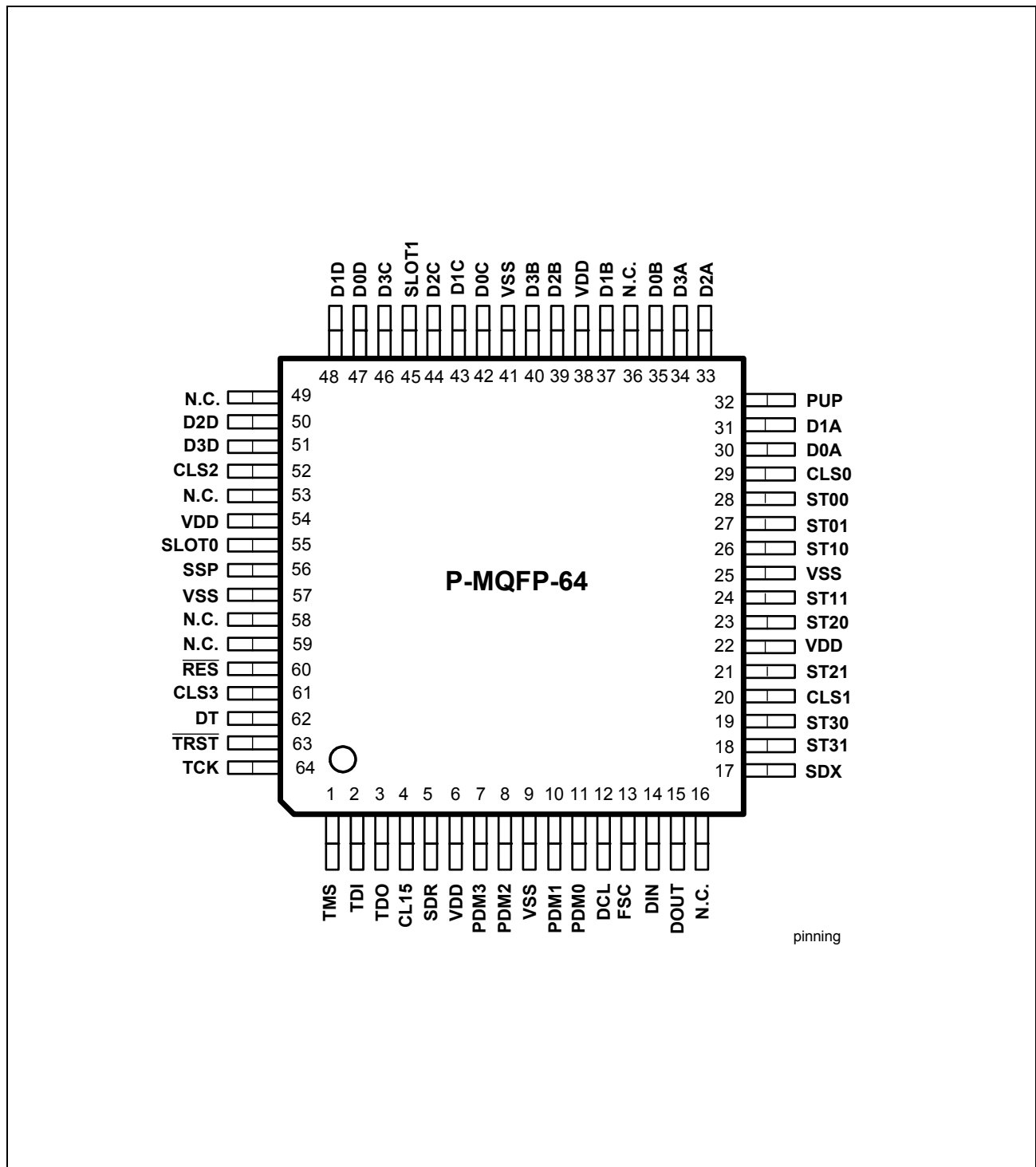
Figure 6   Pin Configuration

2.2 Pin Definitions and Functions

Table 1   Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function

IOM®-2 Interface

Pin No.	Symbol	Input (I) Output (O)	Function
13	FSC	I	Frame Synchronization Clock (8 kHz) the start of the first B1-channel in time-slot 0 is marked, FSC is expected to be '1' for at least two DCL periods.
12	DCL	I	Data Clock clock rate ranges from 2048 to 8192 kHz (1024 to 4096 kBit/s)
14	DIN	I	Data In input of IOM®-2 data synchronous to DCL clock
15	DOUT	O (OD/PuP)	Data Out output of IOM®-2 data synchronous to DCL clock

Mode Selection Pins

Pin No.	Symbol	Input (I) Output (O)	Function
60	RES	I	Reset triggers asynchronous HW reset, Schmitt trigger input '1'= inactive '0'= active (see **Table 3**)
55	SLOT0	I	IOM®-2 Channel Slot Selection 0 assigns IOM®-2 channels in blocks of 4 SLOT1, 0: '00'= IOM®-2 channels 0 to 3 '01'= IOM®-2 channels 4 to 7 '10'= IOM®-2 channels 8 to 11 '11'= IOM®-2 channels 12 to 15

Table 1   **Pin Definitions and Functions** (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
45	SLOT1	I (PD)	IOM®-2 Channel Slot Selection 1 assigns IOM®-2 channels in blocks of 4
32	PUP	I (PD)	Push Pull Mode in push pull mode '0' and '1' is actively driven during an occupied time slot outside the active time slots DOUT is high impedance (tristate) '1'= configures DOUT as push/pull output '0'= configures DOUT as open drain output
56	SSP	I	Send Single Pulses (SSP) Test Mode enables/disables SSP test mode '1'= SSP test mode enabled, +1 pulses are issued at the four line ports in 1ms intervals '0'= SSP test mode disabled This pin function corresponds to the SW selection by C/I= SSP besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line *Note: For activation of SSP test mode, pin $\overline{RES}$ and pin DT must be inactive (see* **Table 3***)*
62	DT	I	Data Through (DT) Test Mode enables/disables DT test mode '1'= DT test mode enabled, the U-transceiver is forced on all line ports to enter the 'Transparent' state '0'= DT test mode disabled This pin function corresponds to the SW selection by C/I= DT besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line *Note: For activation of DT test mode, pin $\overline{RES}$ and pin SSP must be inactive (see* **Table 3***)*

Table 1   Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Interface to the Analog Front End			
4	CL15	I	15.36 MHz Master Clock Input
11	PDM0	I	Pulse Density Modulated Receive Data of Line Port 0 pulse density modulated bit stream from the PEB 24902 Quad AFE that is output from the second-order sigma-delta ADC
10	PDM1	I	Pulse Density Modulated Receive Data of Line Port 1 pulse density modulated bit stream from the PEB 24902 Quad AFE that is output from the second-order sigma-delta ADC
8	PDM2	I	Pulse Density Modulated Receive Data of Line Port 2 pulse density modulated bit stream from the PEB 24902 Quad AFE that is output from the second-order sigma-delta ADC
7	PDM3	I	Pulse Density Modulated Receive Data of Line Port 3 pulse density modulated bit stream from the PEB 24902 Quad AFE that is output from the second-order sigma-delta ADC
5	SDR	I	Serial Data Receive Line interface signal from the PEB 24902 Quad AFE that transports level detect information for the wake-up recognition of all 4 lines

Table 1   Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
17	SDX	O	Serial Data Transmit Line interface to the PEB 24902 Quad AFE for the transmit and control data. Transmission is based on clock CL15 (15.36 Mbit/s). For each line port the following bits are exchanged: TD0, TD1: Transmit data RANGE: Range select LOOP: Analog loopback switch PDOW: Power down/power up Synchronization information

Relay Driver/ Status Pins

Pin No.	Symbol	Input (I) Output (O)	Function
30, 35, 42, 47	D0A D0B D0C D0D	O	Relay Driver Pins of Line Port 0 addressable via MON-8 command in IOM$^{®}$-2 channel 0/4/8/12. The logic values of the bit positions A,B,C, D of the MON-8 command 'SETD' determine the output setting. Default value after pin-reset is low. C/I-code reset does not affect the current status.
31, 37, 43, 48	D1A D1B D1C D1D	O	Relay Driver Pins of Line Port 1 addressable via MON-8 command in IOM$^{®}$-2 channel 1/5/9/13. The logic values of the bit positions A,B,C, D of the MON-8 command 'SETD' determine the output setting. Default value after pin-reset is low. C/I-code reset does not affect the current status.
33, 39, 44, 50	D2A D2B D2C D2D	O	Relay Driver Pins of Line Port 2 addressable via MON-8 command in IOM$^{®}$-2 channel 2/6/10/14. The logic values of the bit positions A,B,C, D of the MON-8 command 'SETD' determine the output setting. Default value after pin-reset is low. C/I-code reset does not affect the current status.

Table 1   Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
34, 40, 46, 51	D3A D3B D3C D3D	O	Relay Driver Pins of Line Port 3 addressable via MON-8 command in IOM$^{®}$-2 channel 3/7/11/15. The logic values of the bit positions A,B,C, D of the MON-8 command 'SETD' determine the output setting. Default value after pin-reset is low. C/I-code reset does not affect the current status.
28, 27	ST00 ST01	I	Status Pin of Line Port 0 change of status is passed to IOM$^{®}$-2 channel 0/4/8/12 via the MON-8 message 'AST' at bit positions S_0, S_1. Connect to either VDD or VSS if not used.
26, 24	ST10 ST11	I	Status Pin of Line Port 1 change of status is passed to IOM$^{®}$-2 channel 1/5/9/13 via the MON-8 message 'AST' at bit positions S_0, S_1. Connect to either VDD or VSS if not used.
23, 21	ST20 ST21	I	Status Pin of Line Port 2 change of status is passed to IOM$^{®}$-2 channel 2/6/10/14 via the MON-8 message 'AST' at bit positions S_0, S_1. Connect to either VDD or VSS if not used.
19, 18	ST30 ST31	I	Status Pin of Line Port3 change of status is passed to IOM$^{®}$-2 channel 3/7/11/15 via the MON-8 message 'AST' at bit positions S_0, S_1. Connect to either VDD or VSS if not used.

Test Pins

29	CLS0	O	Clock of 1 ms period to indicate the received frame of Port 0 can be used for monitoring and test purposes
20	CLS1	O	Clock of 1 ms period to indicate the received frame of Port 1 can be used for monitoring and test purposes

Table 1 **Pin Definitions and Functions** (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
52	CLS2	O	Clock of 1 ms period to indicate the received frame of Port 2 can be used for monitoring and test purposes
61	CLS3	O	Clock of 1 ms period to indicate the received frame of Port 3 can be used for monitoring and test purposes
49	N.C.	I	No function May be clamped to ground for compatibility to former versions.
53	N.C.	I	No function May be clamped to VDD for compatibility to former versions.

JTAG Boundary Scan

Pin No.	Symbol	Input (I) Output (O)	Function
64	TCK	I	Test Clock[1]
1	TMS	I (PU)	Test Mode Select
2	TDI	I (PU)	Test Data Input
3	TDO	O	Test Data Output
63	$\overline{\text{TRST}}$	I (PU)	JTAG Boundary Scan Disable resets the TAP controller state machine (asynchronous reset), active low. Clamp $\overline{\text{TRST}}$ to GND if the Boundary Scan logic is not used '1'= reset inactive '0'= reset active

Power Supply Pins

Pin No.	Symbol		Function
6, 22, 38, 54	VDD		3.3 V ±0.3 V supply voltage
9, 25, 41, 57	VSS		0 V ground

[1] In case that JTAG is reset via $\overline{\text{TRST}}$ = 0, pin TCK shall be pulled to either power or ground, e.g. with a pull-down of 47 kΩ.

OD: Open Drain
PuP: Push Pull
PD: Internal Pull Down (e.g. 10 to 20 kΩ)
PU: Internal Pull Up (e.g. 10 to 20 kΩ)

2.3 Pinning Changes from DFE-T V1.2 to DFE-T V2.2

Table 2   Pinning Changes

Pin No.	V2.2	V1.2	Comment
29, 20, 52, 61	CLS0, 1, 2, 3	CLS0 1, 2, 3	Clock of **1 ms** Period to indicate the received frame of Port 0, 1, 2, 3 (before: 120 kHz Transmit Baud Clock)
32	PUP	SLOT2	additional push-pull mode for pin DOUT eases interface adaption, SLOT2 was not used in V1.2
45	SLOT1	N.C.	increased max data rate (4 MBit/s) requires an additional SLOT pin
49	N.C.	TP3	no function
53	N.C.	LT	as in V1.x LT-RP mode is neither supported in V2.2
55	SLOT0	SLOT	renamed
56	SSP	TSP	dedicated pin for 'Send Single Pulses' test mode
62	DT	TP2	dedicated pin for 'Data Through' test mode
63	$\overline{\text{TRST}}$	TP1	power-on-reset is replaced by a dedicated reset line

Pin-Controlled Test Modes

Table 3   Pin Controlled Test Modes with DFE-T V2.2

Mode	$\overline{\text{RES}}$ Pin	SSP Pin	DT Pin
Reset (Master Reset)	0	don't care	don't care
Data-Through	1	0	1
Send-Single-Pulses	1	1	0
Undefined	1	1	1

3 Functional Description

3.1 Functional Overview

A functional overview of the DFE-T V2.2 is given in **Figure 7**. Besides the signal processing and frame formatting blocks the PEF 24901 features an on-chip activation/deactivation controller and programmable general purpose I/O pins for the control of test relays and power feeding circuits. An application specific DSP core services all four lines and cuts chip size to a minimum.
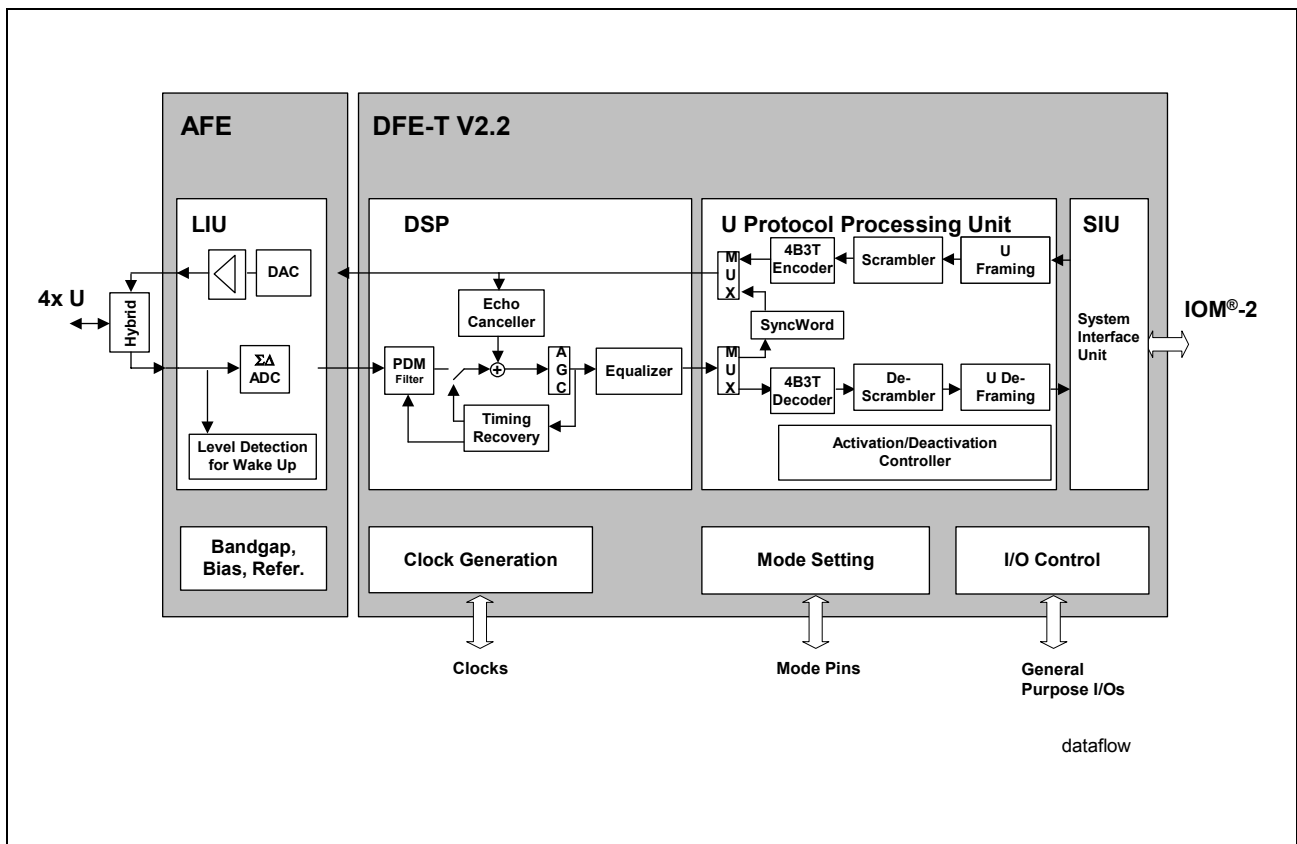
Figure 7   Block Diagram and Data Flow Diagram (DFE-T V2.2 + AFE V2.1)

3.2 IOM®-2 Interface

The IOM®-2 interface is a four-wire serial interface providing a symmetrical full-duplex communication link to layer-1 and layer-2 backplane devices. It transports user data, control/programming and status information via dedicated time multiplexed channels.

The structure used follows the 2B + 1 D-channel structure of ISDN. The ISDN-user data rate of 144 kbit/s (B1 + B2 + D) on the U-interface is transmitted transparently in both directions (U <=> IOM®) over the interface.
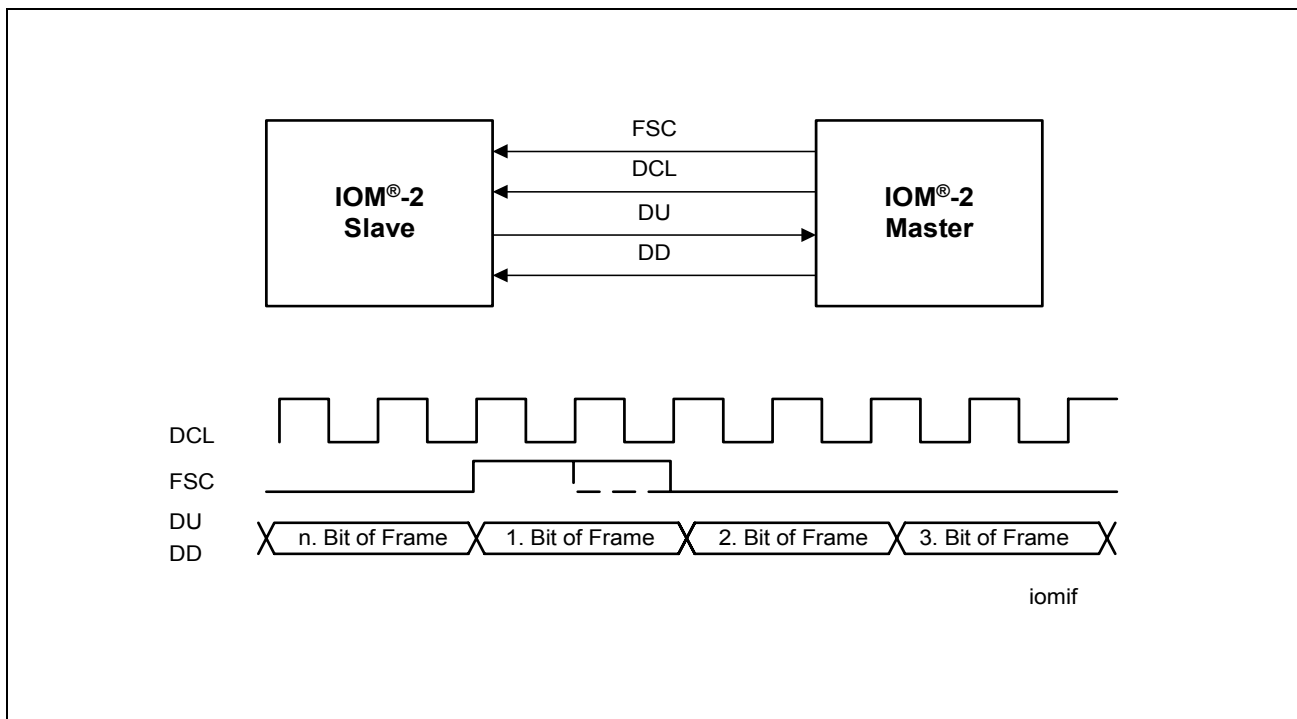
Figure 8   Clock Supply and Data Exchange between Master and Slave

The **Frame Sync Signal FSC** is a 8 kHz signal delimiting the frames. This signal is used to determine the start of a frame.

The data is clocked by a **Data Clock (DCL)** which operates at twice the data rate. The data clock is a square wave signal with a duty cycle ratio of typically 1:1. Incoming data is sampled on the falling edge of the DCL-clock.

Data is carried over **Data Upstream (DD)** and **Data Downstream (DU)** signals. The upstream and downstream directions are always defined with respect to the exchange: Downstream refers to information flowing from the exchange to the subscriber, upstream is defined vice versa.

The output line is operating either as open drain or push-pull output. Both modes are selected by signal "PUP". In open drain mode an external pull-up resistor is required. The absence of a pull-up resistor is not automatically recognized (i.e. no push-pull detection).

Within one FSC-period, 128 to 512-bit are transmitted, corresponding to DCL-frequencies ranging from 2048 kHz up to 8192 kHz. The following table shows possible operating frequencies of the IOM$^®$-2-interface.

Table 4   IOM$^®$-2 Data Rates

DCL Frequency [kHz]	Data Rate [kBit/s]	IOM$^®$-2 Channels
2048	1024	4
3072	1536	6
4096	2048	8
6144	3072	12
8192	4096	16

3.2.1   IOM$^®$-2 Interface Frame Structure

The typical IOM$^®$-2 line card application comprises a DCL-frequency of 4096 kHz with a nominal bit rate of 2048 kbit/s. Therefore eight channels are available, each consisting of the basic frame with a nominal data rate of 256 kbit/s. The downstream data (DD) is transferred on signal DIN, the upstream data (DU) on signal DOUT. The IOM$^®$-2 channel assignment is programmable by pin strapping (SLOT1,0).

The basic IOM$^®$-2 frame and clocking structure consists of:

channel bits	B1	B2	Monitor	D	Command / Indicate	MR	MX
	8	8	8	2	4	1	1

- Two 64-kbit/s channels B1 and B2
- The monitor channel for transferring maintenance information between layer-1 and layer-2 devices
- Two bits for the 16-kbit/s D-channel
- Four command / indication (C/I) bits for controlling of layer-1 functions (activation/ deactivation and additional control functions) by the layer-2 controller
- Two bits MR and MX for handling the monitor channel
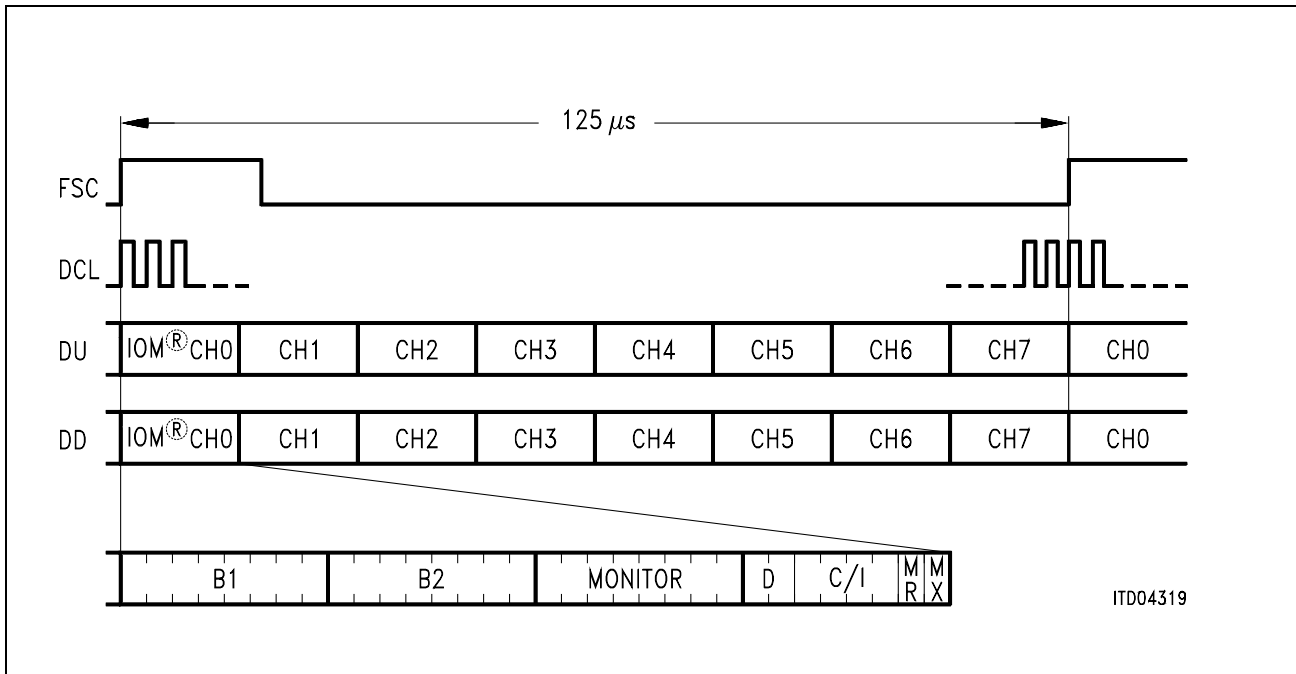
Figure 9   Multiplexed Frame Structure of the IOM®-2 Interface

3.2.2   IOM®-2 Command/ Indicate Channel

The Command/Indication (C/I) channel carries real-time control and status information between the DFE-T V2.2 and a layer-1 control device. A new C/I code must be detected in six consecutive IOM®-2 frames to be considered valid, unconditional commands (i.e. RES, SSP, DT and commands in the states "Test" and "Reset") must be applied up to 2 ms before they are recognized. An indication is issued permanently by the DFE-T V2.2 on DOUT until a new indication needs to be forwarded.

The C/I code is 4-bit wide and located at bit positions 27–30 in each time-slot. A listing and explanation of the U-transceiver C/I codes can be found on page 3-54.

3.2.3   IOM®-2 Monitor Channel

The Monitor channel represents a second method of initiating and reading U-transceiver specific information. Features of the monitor channel are supplementary to the command/indicate channel. Unlike the command/indicate channel with an emphasis on status control, the monitor channel provides access to internal bits (maintenance, overhead) and test functions (local loop-backs, block error counter etc.).

Besides the known MON-8 commands the new MON-12 commands are introduced in the DFE-T V2.2:

New MON-12 Class

By use of MON-12 commands the DFE-T V2.2 provides the ability to address parts of the device internal register map and thus to address functions that have been added with version 2.2. MON-12 commands are always prioritized and processed first if other Monitor commands are outstanding. See **Chapter 3.2.4** for the details.

This means that Monitor commands are split into two categories. Each category derives its name from the first nibble (4 bits) of the two byte long message. These are:

- MON-12 (Internal Register Map)
- MON-8 (Local Functions)

The various MON-8-commands are discussed in detail in chapter **Chapter 5**.

Structure

The structure of the Monitor channel is 8-bit wide, located at bit position 17 – 24 in every time-slot. Monitor commands/messages sent to/from the U-transceiver are always 2 bytes long.

Transmission of multiple monitor bytes is specified by IOM®-2 (see next section "Handshake Procedure" for details). For handshake control in multiple byte transfers, bit 31, monitor read "MR", and bit 32, monitor transmit "MX", of every time-slot are used.

Verification

A double last-look criterion is implemented for the monitor channel. If the monitor message that was received consecutively after a change has been detected is not identical to the message that was received before the message will be aborted.

Handshake Procedure

IOM®-2 provides a sophisticated handshake procedure for the transfer of monitor messages. For handshake control two bits, MX and MR, are assigned to each IOM®-2 frame (on DIN and DOUT). The monitor transmit bit (MX) indicates when a new byte has been issued in the monitor channel (active low). The transmitter postpones transmitting the next information until the correct reception has been confirmed. A correct reception will be confirmed by setting the monitor read bit (MR) to low.

The monitor channel is full duplex and operates on a pseudo-asynchronous base, i.e. while data transfer on the bus takes place synchronized to frame synchronization, the flow of monitor data is controlled by the MR- and MX-bits. Monitor data will be transmitted repeatedly until its reception is acknowledged.

Figure 10 illustrates a monitor transfer at maximum speed. The transmission of a 2-byte monitor command followed by a 2-byte response requires a minimum of 16 IOM®-2 frames (reception 8 frames + transmission 8 frames = 1.875 ms). In case the controller is able to confirm the receipt of first response byte in the frame immediately following the

MX-transition on DOUT from high to low (marker 8 in **Figure 10**), 1 byte may be saved (8 frames + 7 frames).

Transmission and reception of monitor messages can be performed simultaneously by the U-transceiver. In the procedure depicted in **Figure 10** it would be possible for the U-transceiver to transmit monitor data in marker 1–4 (excluding EOM-indication) and receive monitor data from marker 7 onwards.

M 1/2:Monitor message 1. and 2. byte
R 1/2:Monitor response 1. and 2. byte
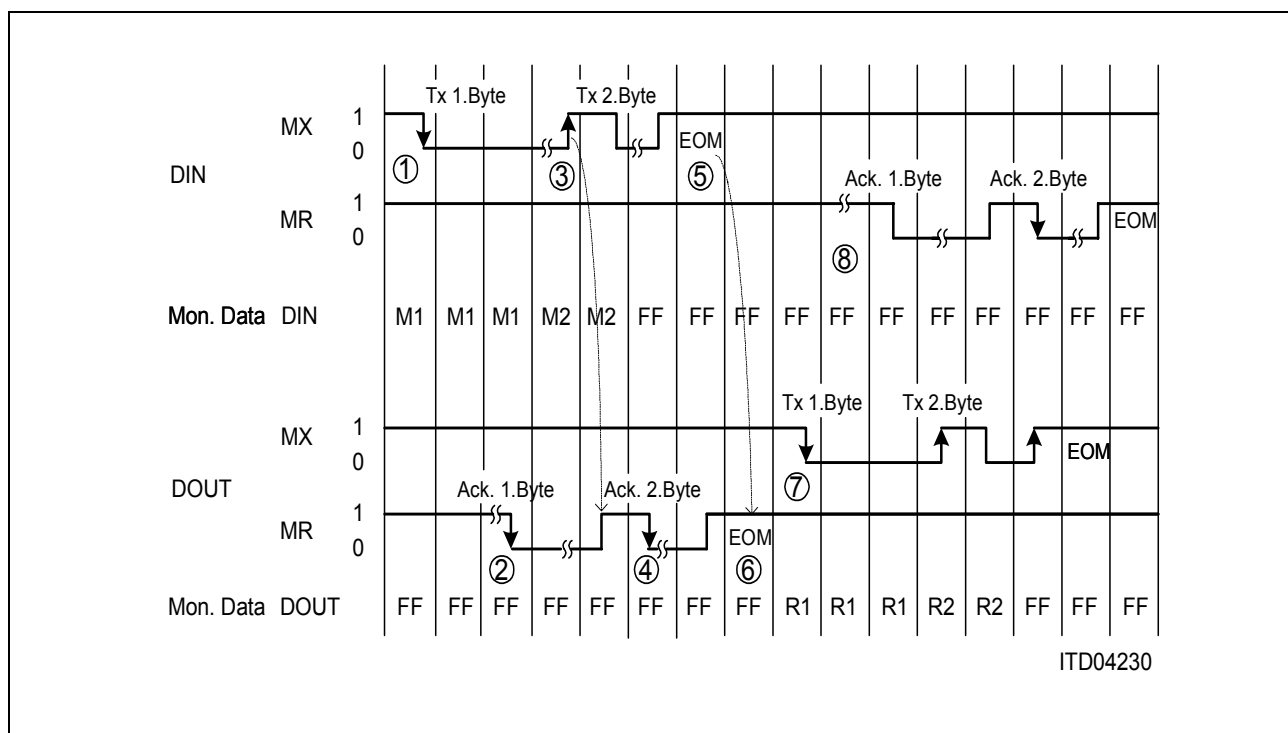
Figure 10   Handshake Protocol with a 2-Byte Monitor Message/Response

Idle State

After the bits MR and MX have been held inactive (i.e. high) for two or more successive IOM®-frames, the channel is considered idle in this direction.

Standard Transmission Procedure

1. The first byte of monitor data is placed by the external controller on the DIN line of the DFE-T V2.2 and MX is activated (low; marker 1 in **Figure 10**).
2. The DFE-T V2.2 reads the data of the monitor channel and acknowledges by setting the MR-bit of DOUT active (marker 2 in **Figure 10**):
   - in the third IOM-2 frame if the transmitted bytes are identical in first and second received frame
   - or later if for instance the double last look criterion is not fulfilled within the first and second receiver frame

3. The second byte of monitor data is placed by the controller on DIN and the MX-bit is set inactive for one single IOM®-frame. This is performed at a time convenient to the controller (marker 3 in **Figure 10**).

4. The DFE-T V2.2 latches the new data byte in the frame, where the rising edge of MX has been detected. In the frame immediately following the MX-transition active-to-inactive, the MR-bit of DOUT is set inactive. If double last look is fulfilled, then the receiver will make a MR-transition inactive-to-active exactly one IOM®-frame later, which the external controller will regard as acknowledgement (marker 4 in **Figure 10**). Else the receiver will sent an Abort Request.

5. After both monitor data bytes have been transferred to the DFE-T V2.2, the controller transmits "End Of Message" (EOM) by setting the MX-bit inactive for two or more IOM®-frames (marker 5 in **Figure 10**).

6. In the frame following the transition of the MX-bit from active to inactive, the DFE-T V2.2 sets the MR-bit inactive (as was the case in step 4). As it detects EOM, it keeps the MR-bit inactive (marker 6 in **Figure 10**). The transmission of the 2 byte monitor command by the controller is complete. In case of a three byte message, the transmission of the 3rd byte is similar to the procedure described in points 3 – 5.

7. If the DFE-T V2.2 is requested to return an answer it will commence with the response as soon as possible. **Figure 10** illustrates the case where the response can be sent immediately (marker 7 in **Figure 10**).

   The procedure for the response is similar to that described in points 1 – 6 except for the transmission direction.

   Transmission of the 2nd monitor byte will be started by the DFE-T V2.2 in the frame immediately following the acknowledgment of the first byte. The U-transceiver does not delay the monitor transfer.

Transmission Abortion

If no EOM is detected after the first two monitor bytes, or received bytes are not identical in the first two received frames, transmission will be aborted through receiver by setting the MR-bit inactive for two or more IOM®-2-frames. The controller reacts with EOM. This situation is illustrated in **Figure 11**.
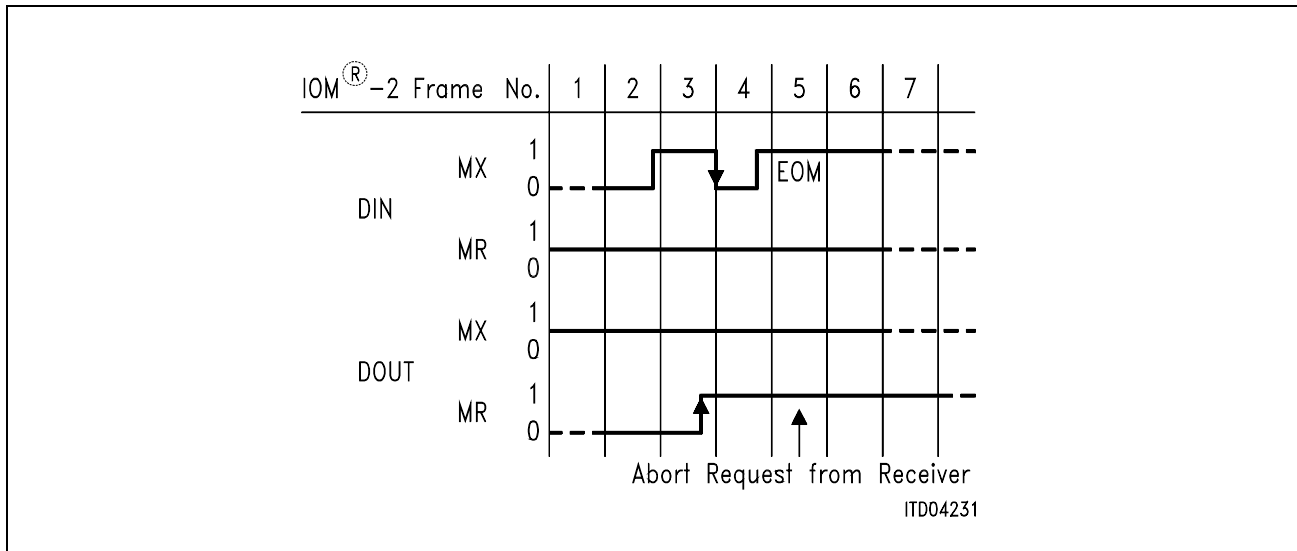
Figure 11   Abortion of Monitor Channel Transmission

3.2.4   MON-12 Protocol

MON-12 commands feature direct access to the device internal register map via the Monitor channel. This means that although the DFE-T V2.2 features no microcontroller interface internal register functions can be directly addressed by use of MON-12 commands.

A MON-12 read request command must be first acknowledged by the DFE-T V2.2 before a subsequent read request can be triggered. In case of a failure condition the DFE-T V2.2 repeats the last outstanding MON-12 answer. MON-12 commands are prioritized over the other MON classes.

If U-interface functions are addressed then the value of register LP_SEL determines the register bank of the channel that is referred to. As a result the desired line port number must be programmed first in register LP_SEL before any U-interface register can be accessed. For this reason MON-12 commands may not be issued simultaneously on different IOM®-2 channels, but must be issued consecutively if they address U-interface functions.

For registers that are addressable by MON-12 commands please refer to the register map in **Chapter 6.2**.

MON-12 commands are of the following format:

• A MON-12 **write command** comprises 3 bytes, the first byte contains the MON-12 header, the second byte the register address, the third byte the register value.
• A MON-12 **read request command** comprises 2 bytes, the first byte contains the MON-12 header, the second byte the register address of the data that is requested.

1. Byte		2. Byte		3. Byte	
1100	w=1 0 0 0	A A A A	A A A A	D D D D	D D D D
MON-12		Register Address		Register Value	

1. Byte		2. Byte	
1100	r=0 0 0 0	A A A A	A A A A
MON-12		Register Address	

- After a read request the DFE-T V2.2 reacts with a 3-byte message. A MON-12 **read answer** comprises 3 bytes, the first byte contains the MON-12 header, the second byte the register address, the third byte the register value.

1. Byte		2. Byte		3. Byte	
1100	r=0 0 0 0	A A A A	A A A A	D D D D	D D D D
MON-12		Register Address		Register Value	

3.3 Interface to the Analog Front End

The interface to the PEF 24902 AFE V2.2 is a 6-wire interface (see **Figure 12**). On SDX and SDR transmit and receive data is exchanged as well as control information for the start-up procedure by means of time division multiplexing.

On **SDX** transmit data, power-up/down information, range function and analog loopback requests are transferred.

On **SDR** level status information is received for all line ports.

On **PDM0..PDM3** the ADC output data from the AFE is transferred to the DFE-T V2.2. The timing of all signals is based on the 15.36 MHz master clock which is provided by the AFE.
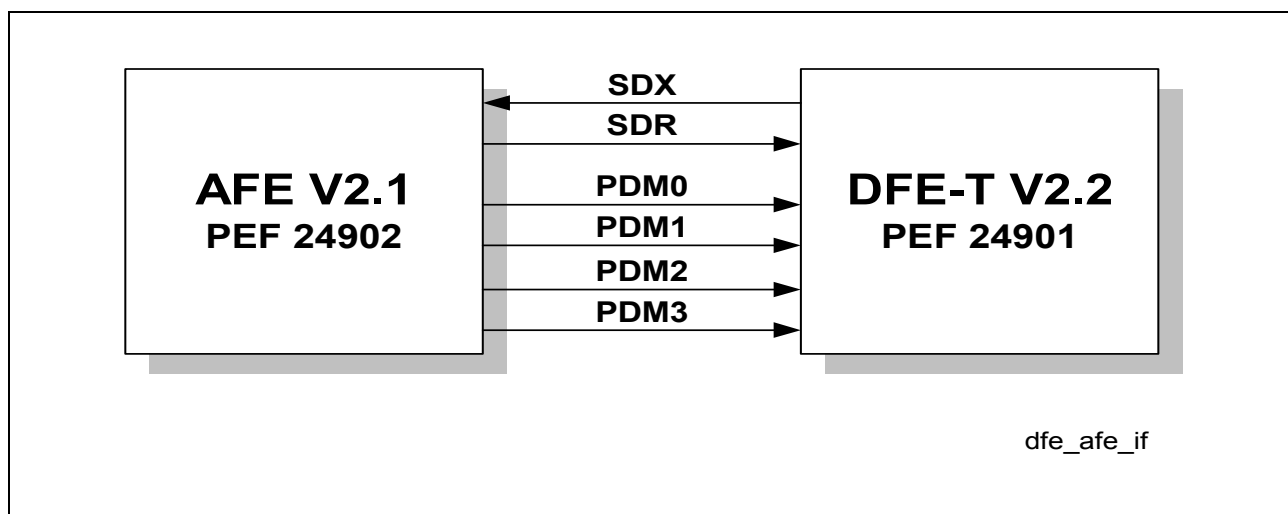
Figure 12   Interface to the Analog Front End

The 128 available bits (related to the 15.36 MHz clock) on SDR/SDX during a 120 kHz period are divided into 9 time-slots. 8 time-slots are 13-bits long and are reserved for data transmission, 1 time-slot is 24-bits long and used for synchronization purposes. The DFE-T V2.2 uses four of them, time-slots no. 1, 3, 5 and 7. **Table 5** shows the assignment of the IOM®-2 channels to the time-slots on SDX/SDR and the assignment of the time-slots to the line ports.

Table 5   Assignments of IOM® Channels to Time-Slots No. on SDX/SDR and Line Ports No.

IOM®-2 Channel No.	Time-Slot No.	Line Port No.
0/4/8/12	1	0
1/5/9/13	3	1
2/6/10/14	5	2
3/7/11/15	7	3

The status on SDR is synchronized to SDX. Each time-slot on SDR carries the corresponding LD bit during the last 12 bits of the slot.
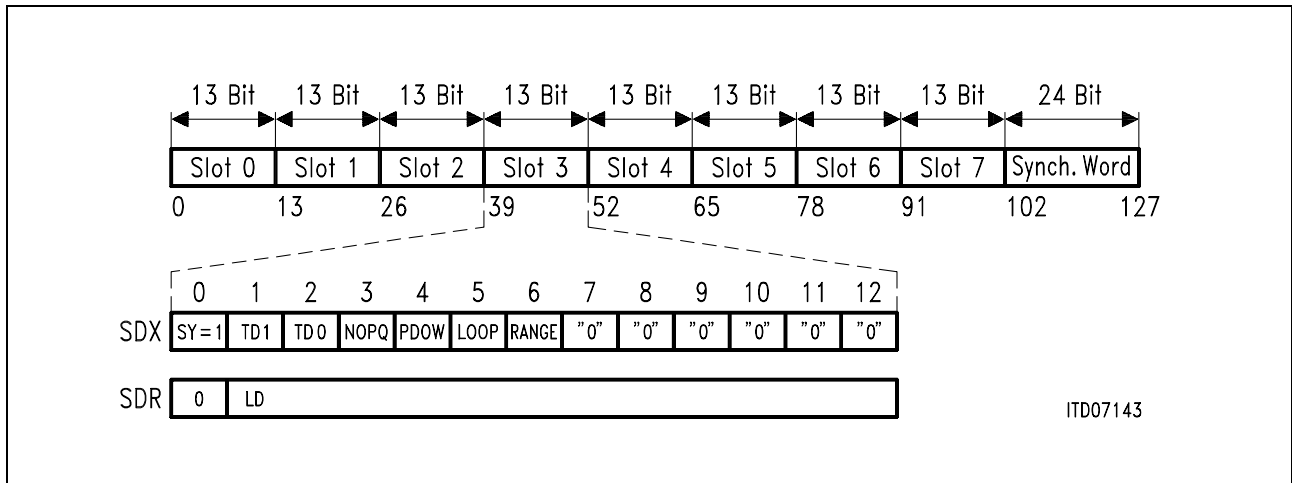
Figure 13   Frame Structure on SDX/SDR

The data on **SDX** is interpreted as follows:

$\overline{\text{NOP}}$:   The $\overline{\text{NOP}}$ bit is always set to '1'.

PDOW: If the PDOW bit is set to '1', the assigned line port is switched to power down. Otherwise it is switched to power-up.

RANGE: RANGE = '1' activates the range function, otherwise the range function is deactivated. "Range function activated" refers to high input levels.

LOOP: LOOP = '1' activates the loop function, i.e. the loop is closed. Otherwise the line port is in normal operation.

SY: First bit of the time-slots with transmission data. For synchronization and bit allocation on SDX, SY is set to '1' on SDX and '0' on SDR.

"0":   Reserved bit. Reserved bits are currently not defined and shall be set to '0'. Some of these bits may be used for test purposes or can be assigned a function in later versions.

The 4B3T data is coded with the bits TD1, TD0:

Table 6   Coding of the 4B3T Data Pulse (AOUT/BOUT)

4B3T Data Pulse	TD1	TD0
0	0	0
+ 1	1	0
− 1	1	1

The data on **SDR** is interpreted as follows:

LD: The level detect information is communicated to the DFE-T V2.2 on SDR. If the signal amplitude reaches the wake-up level, the LD bit toggles with the signal frequency. If the input signal at the U-interface is below the wake-up level, the LD bit is tied to either low or high.

SY: First bit of the time-slots with transmission data. For synchronization and bit allocation on SDX, SY is set to '1' on SDX and '0' on SDR.

Note: After reset , the interface to the analog frontend is activated with reception of FSC clock. If after activation the FSC is no more delivered, the interface to the analog front end keeps running.

3.4 General Purpose I/Os

The DFE-T V2.2 features 6 general purpose I/O pins per line port. This way transparent control of test relays and power feeding circuits is possible via the IOM$^{®}$-2 Monitor channel. Four of the six pins are outputs, two are inputs.

Setting Relay Driver Pins

Four relay driver output pins Dij (where i = 0, 1, 2, 3 denotes the line port no. and j = A, B, C, D specifies the pin) are available per line port. The logic state of the four relay driver outputs which are assigned to the same line port can be set by a single MON-8 command, called 'SETD'. The value is latched as long as no other SETD command with different relay driver settings is received.

The state of the relay driver pins is not affected by any software reset (C/I= RES). The state of all relay driver pins after hardware reset is „low".

Reading Status Pins

Each line port owns two status pins ST$_{ij}$ (where i = 0,1, 2, 3 denotes the line port no. and j = 0, 1 specifies the pin) whose logical value is reported in the associated Monitor channel. Any signal change at one of the status pins ST1..4 causes automatically the issue of a two-byte MON-8 message 'AST' whose two least significant bits reflect the status of pin STij.

However, this automatic mechanism is only enabled again, if the previous status pin message has been transferred and acknowledged correctly according to the Monitor channel handshake protocol. It takes the DFE-T V2.2 at least 8x IOM$^{®}$-2 frames (1 ms) to transmit the 2-byte MON-8 message. Thus, repeated changes within periods shorter than 8x IOM$^{®}$-2 frames will overwrite the status pin register information. For this reason only the value of the last recent status change will be reported. Note that the MON-8 transfer time depends also on the reaction time (acknowledge by MR-bit) of the DFE-T counterpart.

Besides this automatic report the DFE-T V2.2 will issue the status pin Monitor message 'AST' upon the MON-8 request 'RST' .

The ST$_{ij}$ pins have to be tied to either VDD or GND, if they are not used.

3.5 U-Transceiver Functions

The 4B3T U-interface performs full duplex data transmission and reception at the U-reference point according to ETSI TS102080 and FTZ 1TR 220. It applies the 4B3T block code together with adaptive echo cancelling and equalization. Transmission performance shall be such that it meets all ETSI and FTZ test loops with margin.

The U-interface is designed for data transmission on twisted pair wires in local telephone loops with ISDN basic rate access and a user bit rate of 144 kbit/s.

The following information is transmitted over the twisted pair:

- Bidirectional:
  - B1, B2, D data channels
  - 120 kHz Symbol clock, 160 kbit/s Transmission rate
  - 1 kHz Frame
  - Activation
- From LT to NT side:
  - Power feeding
  - Deactivation
  - Remote control of test loops
- From NT to LT side:
  - Indication of monitored code violations

On the U-interface transmission ranges of 4.2 km on wires of 0.4 mm diameter wires are achieved without additional signal regeneration in the loop. The transmission ranges can be doubled by inserting a repeater for signal regeneration.

3.5.1   4B3T Frame Structure

1 ms frames are transmitted across the U-interface, each consisting of:

- 108 symbols: 144-bit scrambled and coded B1 + B2 + D data
- 11 symbols: Barker code for both symbol and frame synchronization (not scrambled)
- 1 symbol: Ternary maintenance symbol (not scrambled)

The 108 user data symbols are split into four equally structured groups. Each group (27 ternary symbols, resp. 36 bits) contains the user data of two IOM$^{®}$-2 frames in the same order (8B + 8B + 2D + 8B + 8B + 2D).

Different syncwords are used for each direction:

- Downstream from LT to NT $+ + + - - - + - - + -$
- Upstream from NT to LT $- + - - + - - - + + +$

On the NT side the transmitted Barker code begins 60 symbols after the received Barker code and vice versa.

Table 7   Frame Structure for Downstream Transmission LT to NT

1	2	3	4	5	6	7	8	9	10	11	12
D_1	D_1	D_1	D_1	D_1	D_1	D_1	D_1	D_1	D_1	D_1	D_1
13	14	15	16	17	18	19	20	21	22	23	24
$D_{1/2}$	$D_{1/2}$	$D_{1/2}$	D_2	D_2	D_2	D_2	D_2	D_2	D_2	D_2	D_2
25	26	27	28	29	30	31	32	33	34	35	36
D_2	D_2	D_2	D_3	D_3	D_3	D_3	D_3	D_3	D_3	D_3	D_3

Table 7   Frame Structure for Downstream Transmission LT to NT (cont'd)

37 D_3	38 D_3	39 D_3	40 $D_{3/4}$	41 $D_{3/4}$	42 $D_{3/4}$	43 D_4	44 D_4	45 D_4	46 D_4	47 D_4	48 D_4
49 D_4	50 D_4	51 D_4	52 D_4	53 D_4	54 D_4	55 D_5	56 D_5	57 D_5	58 D_5	59 D_5	60 D_5
61 D_5	62 D_5	63 D_5	64 D_5	65 D_5	66 D_5	67 $D_{5/6}$	68 $D_{5/6}$	69 $D_{5/6}$	70 D_6	71 D_6	72 D_6
73 D_6	74 D_6	75 D_6	76 D_6	77 D_6	78 D_6	79 D_6	80 D_6	81 D_6	82 D_7	83 D_7	84 D_7
85 **M**	86 D_7	87 D_7	88 D_7	89 D_7	90 D_7	91 D_7	92 D_7	93 D_7	94 D_7	95 $D_{7/8}$	96 $D_{7/8}$
97 $D_{7/8}$	98 D_8	99 D_8	100 D_8	101 D_8	102 D_8	103 D_8	104 D_8	105 D_8	106 D_8	107 D_8	108 D_8
109 D_8	110 **+**	111 **+**	112 **+**	113 **−**	114 **−**	115 **−**	116 **+**	117 **−**	118 **−**	119 **+**	120 **−**

D_1 ... D_8 Ternary 2B + D data of IOM-2 frames 1 ... 8
M   Maintenance symbol
+, −   Syncword

Table 8   Frame Structure for Upstream Transmission NT to LT

1 U_1	2 U_1	3 U_1	4 U_1	5 U_1	6 U_1	7 U_1	8 U_1	9 U_1	10 U_1	11 U_1	12 U_1
13 $U_{1/2}$	14 $U_{1/2}$	15 $U_{1/2}$	16 U_2	17 U_2	18 U_2	19 U_2	20 U_2	21 U_2	22 U_2	23 U_2	24 U_2
25 **M**	26 U_2	27 U_2	28 U_2	29 U_3	30 U_3	31 U_3	32 U_3	33 U_3	34 U_3	35 U_3	36 U_3
37 U_3	38 U_3	39 U_3	40 U_3	41 $U_{3/4}$	42 $U_{3/4}$	43 $U_{3/4}$	44 U_4	45 U_4	46 U_4	47 U_4	48 U_4
49 U_4	50 **−**	51 **+**	52 **−**	53 **−**	54 **+**	55 **−**	56 **−**	57 **−**	58 **+**	59 **+**	60 **+**
61	62	63	64	65	66	67	68	69	70	71	72

Table 8   Frame Structure for Upstream Transmission NT to LT (cont'd)

U_4	U_4	U_4	U_4	U_4	U_4	U_5	U_5	U_5	U_5	U_5	U_5
73	74	75	76	77	78	79	80	81	82	83	84
U_5	U_5	U_5	U_5	U_5	U_5	$U_{5/6}$	$U_{5/6}$	$U_{5/6}$	U_6	U_6	U_6
85	86	87	88	89	90	91	92	93	94	95	96
U_6	U_6	U_6	U_6	U_6	U_6	U_6	U_6	U_6	U_7	U_7	U_7
97	98	99	100	101	102	103	104	105	106	107	108
U_7	U_7	U_7	U_7	U_7	U_7	U_7	U_7	U_7	$U_{7/8}$	$U_{7/8}$	$U_{7/8}$
109	110	111	112	113	114	115	116	117	118	119	120
U_8	U_8	U_8	U_8	U_8	U_8	U_8	U_8	U_8	U_8	U_8	U_8

U_1 ... U_8 Ternary 2B + D data of IOM-2 frames 1... 8

M   Maintenance symbol

+, -   Syncword

3.5.2   Maintenance Channel

The 4B3T frame structure provides a 1 kbit/s M(aintenance)-channel for the transfer of remote loopback commands, error indications and transparent messages.

Loopback Commands

The LT station uses the M-channel to request remote loopbacks. Loopback commands are coded with a series of '0' and '+' symbols.

- A continuous series of '+0' requests for loopback 1A activation in the repeater
- A continuous series of '+' requests for loopback 2 activation in the NT
- A continuous series of '0' requests for deactivation of any loopback

The NT station reacts as soon as the pattern has been detected in 8 consecutive symbols.

Error Indications

The NT U-transceiver reports line code violations via the M-channel to the exchange by setting one M-Bit to '+' polarity.

Transparent Messages

Transparent messages are not supported.

3.5.3 Coding from Binary to Ternary Data

Each 4 bit block of binary data is encoded into 3 ternary symbols using the MMS 43 block code according to **Table 9**.

The number of the next column to be used, is given at the right hand side of each block. The left hand signal elements in the table (both ternary and binary) are transmitted first.

Table 9   **MMS 43 Coding Table**

				S1				S2				S3				S4			
$t \rightarrow$				$t \rightarrow$				$t \rightarrow$				$t \rightarrow$				$t \rightarrow$			
0	0	0	1	0	–	+	1	0	–	+	2	0	–	+	3	0	–	+	4
0	1	1	1	–	0	+	1	–	0	+	2	–	0	+	3	–	0	+	4
0	1	0	0	–	+	0	1	–	+	0	2	–	+	0	3	–	+	0	4
0	0	1	0	+	–	0	1	+	–	0	2	+	–	0	3	+	–	0	4
1	0	1	1	+	0	–	1	+	0	–	2	+	0	–	3	+	0	–	4
1	1	1	0	0	+	–	1	0	+	–	2	0	+	–	3	0	+	–	4
1	0	0	1	+	–	+	2	+	–	+	3	+	–	+	4	–	–	–	1
0	0	1	1	0	0	+	2	0	0	+	3	0	0	+	4	–	–	0	2
1	1	0	1	0	+	0	2	0	+	0	3	0	+	0	4	–	0	–	2
1	0	0	0	+	0	0	2	+	0	0	3	+	0	0	4	0	–	–	2
0	1	1	0	–	+	+	2	–	+	+	3	–	–	+	2	–	–	+	3
1	0	1	0	+	+	–	2	+	+	–	3	+	–	–	2	+	–	–	3
1	1	1	1	+	+	0	3	0	0	–	1	0	0	–	2	0	0	–	3
0	0	0	0	+	0	+	3	0	–	0	1	0	–	0	2	0	–	0	3
0	1	0	1	0	+	+	3	–	0	0	1	–	0	0	2	–	0	0	3
1	1	0	0	+	+	+	4	–	+	–	1	–	+	–	2	–	+	–	3

3.5.4 Decoding from Ternary to Binary Data

Decoding is done in the reverse manner of coding. The received blocks of 3 ternary symbols are converted into blocks of 4 bits. The decoding algorithm is given in **Table 10**.

As in the encoding table the left hand symbol of each block (both binary and ternary) is the first bit and the right hand is the last. If a ternary block "0 0 0" is received, it is decoded to binary "0 0 0 0". This pattern usually occurs only during deactivation.

Table 10   4B3T Decoding Table

Ternary Block			Binary Block			
0 0 0,	+ 0 +,	0 − 0	0	0	0	0
0 − +			0	0	0	1
+ − 0			0	0	1	0
0 0 +,	− − 0		0	0	1	1
− + 0			0	1	0	0
0 + +,	− 0 0		0	1	0	1
− + +,	− − +		0	1	1	0
− 0 +			0	1	1	1
+ 0 0,	0 − −		1	0	0	0
+ − +,	− − −		1	0	0	1
+ + −,	+ − −		1	0	1	0
+ 0 −			1	0	1	1
+ + +,	− + −		1	1	0	0
0 + 0,	− 0 −		1	1	0	1
0 + −			1	1	1	0
+ + 0,	0 0 −		1	1	1	1

3.5.5   Monitoring of Code Violations

The running digital sum monitor (RDSM) computes the running digital sum from the received ternary symbols by adding the polarity of the received user data (+ 1, 0, −1). At the end of each block, the running digital sum is supposed to reflect the number of the next column in **Table 9 "MMS 43 Coding Table" on Page 48**.

A code violation has occurred if the running digital sum is less than one or more than four at the end of a ternary block, or if the ternary block 0 0 0 (three user symbols with zero polarity) is found in the received data.

If at the end of a ternary block no error was found, the running digital sum retains its current value. If the counter value is greater than 4, it is set to 4 at the beginning of the next ternary block, if its value is 0 or less, it is set to one. So after a code violation has been detected, the RDSM synchronizes itself within a period depending on the received data pattern. Note there are some transmission errors which do not cause a code violation.

3.5.6 Scrambler / Descrambler

Scrambler

The binary transmit data from the IOM$^®$-2 interface is scrambled with a polynomial of 23 bits, before it is sent to the 4B3T coder. The scrambling algorithm ensures that no sequences of permanent binary 0 s or 1 s are transmitted.

– The scrambler polynomial in **LT mode** and **NT mode with the analog loop closed** is:

$$z^{-23} + z^{-5} + 1$$

– The scrambler polynomial in **NT mode with open analog loop** is:

$$z^{-23} + z^{-18} + 1$$

Descrambler

The received data (after decoding from ternary to binary) is multiplied with a polynomial of 23 bits in order to recover the original data before it is forwarded to the IOM$^®$-2 interface. The descrambler itself is synchronized after 23 symbols.

– The descrambler polynomial in **LT mode with open analog loop** is:

$$z^{-23} + z^{-18} + 1$$

– The descrambler polynomial in **NT mode** or in **LT with the analog loop closed** is:

$$z^{-23} + z^{-5} + 1$$

3.5.7 4B3T Signal Elements

For control and monitoring purposes of the activation/deactivation progress the following signal elements are defined by TS 102 080 and FTZ 1 TR 220.

Encoding Scheme

The table below describes the characteristics of the defined 4B3T signal elements.

Table 11   Coding of the 4B3T Signal Elements

Upstream from NT to LT	Downstream from LT to NT
U1W: 16 times ternary + + + + + + + + − − − − − − − − A tone of: Frequency: 7.5 kHz Period: 2.13 ms	U2W 16 times ternary + + + + + + + + − − − − − − − − A tone of: Frequency: 7.5 kHz Period: 2.13 ms
U1A: Binary continuous "0" before scrambling. No frame, ternary "0" instead of Barker code	U2A: Binary continuous "0" before scrambling. No frame, ternary "0" instead of Barker code
U1: Binary continuous "0" before scrambling. Frame (Transmitting Barker code)	U2: Binary continuous "0" before scrambling. Frame (Transmitting Barker code)
U3: Binary continuous "1" before scrambling. Frame (Transmitting Barker code)	U4H: Binary continuous "1" before scrambling with duration of 1 ms. Frame (Transmitting Barker code)
U5: Binary data from the digital interface. Frame (Transmitting Barker code)	U4: Binary data from the digital interface. Frame (Transmitting Barker code)
U0: Ternary continuous "0" No frame, no signal level	U0: Ternary continuous "0" No frame, no signal level

Detection of U0, U1, U2, U3 and U4H

- The DFE-T V2.2 detects an **U1 or U3** signal element if continuous binary '0' or '1', respectively, is found on the descrambler output for at least 8 subsequent U-frames. Thus these signal elements are detected valid after 8 to 9 ms.
- **U4H** is recognized if the NT finds at least 16 subsequent binary 1 s in the data stream.
- **U0** is recognized if the LT finds one complete frame with continuous zero level. The significance of the U0 signal element is given in **Table 12**.

Significance of the 4B3T Signal Elements

Table 12 lists the defined 4B3T signal elements that are exchanged across the U-reference point in the course of an activation or deactivation process.

Table 12   4B3T Signal Elements

U0	No signal or deactivation signal that is used in both directions. Downstream, it requests the NT to deactivate. Upstream, the NT acknowledges by U0 that it is deactivated.
U1W	Awake or awake acknowledge signal **upstream** (7.5 kHz) used in the awake procedure of the U-interface.
U2W	Awake or awake acknowledge signal **downstream** (7.5 kHz) used in the awake procedure of the U-interface.
U2	The LT sends U2 to enable the own echo canceller to adapt the coefficients. By the Barker code the NT at the other end is enabled to synchronize. The detection of U2 is used by the NT as a criterion for synchronization. The M-channel on U may be used to transfer loop commands.
U1A	U1A is similar to U1 but without framing information. While the NT synchronizes on the received signal, it sends out U1A to enable its echo canceller to adapt its coefficients, but sends no Barker code to prevent the LT from synchronizing on the still asynchronous signal. Due to proceeding synchronization, the U-frame may jump from time to time. U1A can not be detected by the far-end LT.
U1	When synchronized, the NT sends the Barker code and the LT may synchronize itself. U1 indicates additionally that a terminal equipment has not yet activated. Upon receiving U1 the LT indicates the synchronized state by C/I 'UAI' to layer-2. Usually during activation, no U1 signal is detected in the LT because the TE is activated first and U1 changes to U3 before being detected. The M-channel on U may be used to transfer code error indications.
U3	U3 indicates that the whole link to the TE is synchronous in both directions. On detecting U3 the LT requests the NT by U4H to establish a fully transparent connection. The M-channel on U may be used to transfer code error indications.

Table 12   4B3T Signal Elements (cont'd)

U4H	U4H requires the NT to go to the 'Transparent' state. On detecting U4H the NT stops sending signal U3 and informs the S-transceiver or a layer-2 device via the IOM®-2 interface. The M-channel on U may be used to transfer loop commands.
U4	U4 transports operational data on B and D channels. The M-channel on U may be used to transfer loop commands.
U5	U5 transports operational data on B and D channels. The M-channel on U may be used to transfer code error indications.
SP	The DFE-T V2.2 sends periodically single pulses once per millisecond on the U-interface. The test mode can be used for pulse mask measurements.

3.5.8   Awake Protocol

For the awake process two signals are defined 'U1W' and 'U2W'. Depending on the call direction (up-, downstream) U1W and U2W are interpreted as awake or acknowledge signals (see figures below).
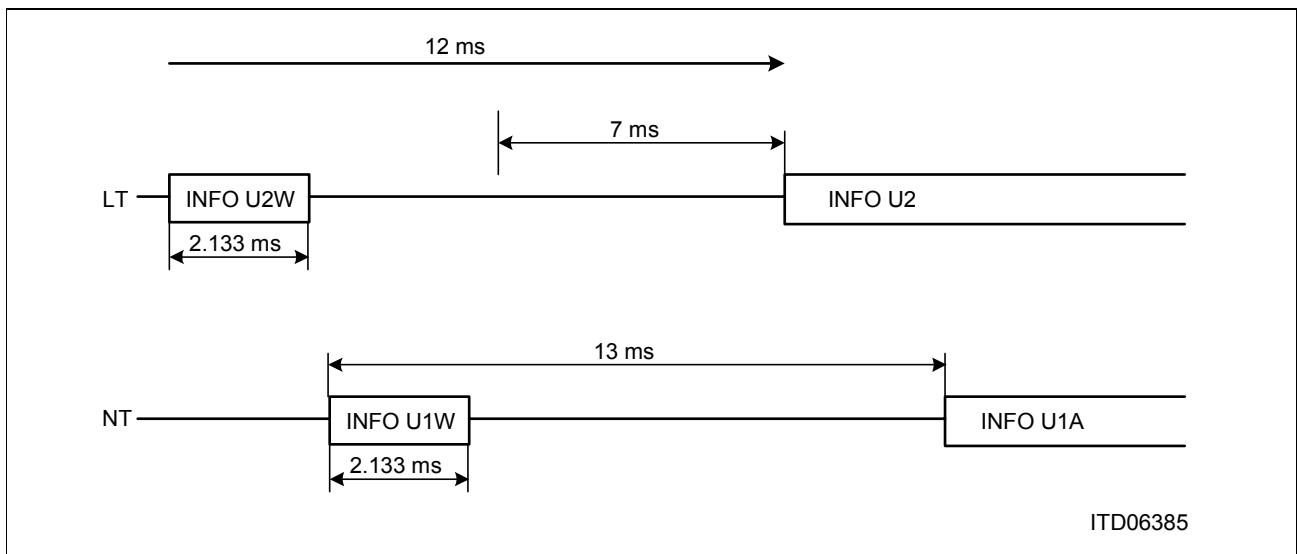
Figure 14   Awake Procedure Initiated by the LT
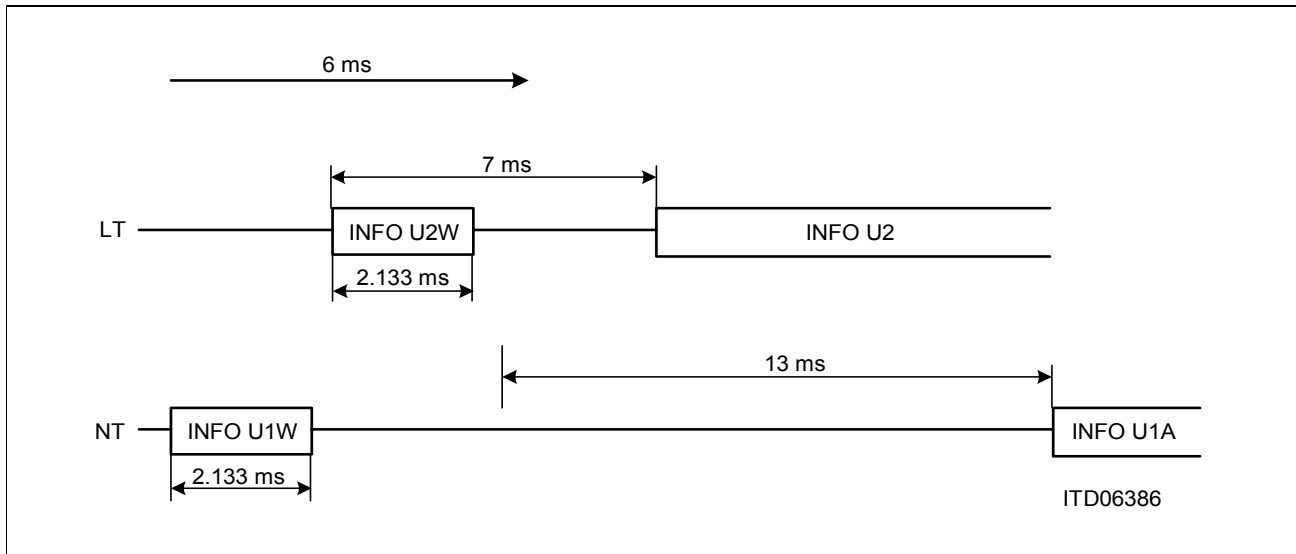
Figure 15   Awake Procedure Initiated by the NT

Acting as Calling Station

After sending the awake signal, the awaking device waits for the acknowledge. After 12 ms the awake signal is repeated, if no acknowledge has been recognized. If an acknowledge signal has been recognized, the DFE-T V2.2 waits for its possible repetition (in case of previous coincidence of two awake signals).

If no repetition was detected, the DFE-T V2.2 starts transmitting U2 with a delay of 7 ms. If such a repetition is detected, the DFE-T V2.2 interprets it as an awake signal and behaves like a device awoken by the far-end.

Acknowledging a Wake-Up Call

If the DFE-T V2.2 detects an awake signal on U, an acknowledge signal is sent out. Afterwards the DFE-T V2.2 waits for a possible repetition of the awake signal (in case the acknowledge signal has not been recognized).

If no repetition is found, the awoken DFE-T V2.2 starts sending U2 after 7 ms from detecting the awake signal. If a repeated awake signal is found, the procedure in the awoken DFE-T V2.2 starts again.

3.5.9   C/I Codes

The Control/Indicate (C/I) channel is used to control the operational status of the DFE-T V2.2 and to issue corresponding indications. The four C/I channels operate completely independently

Table 13 presents all defined C/I codes (former C/I code names of the DFE-T V1.2 are given in brackets).

A new command or indication will be recognized valid after it has been detected in two to five successive IOM®-frames (Unconditional commands must be applied up to 2 ms before they are recognized). Indications are strictly state orientated. Refer to the state diagram in the following section for commands and indications applicable in various states.

Commands have to be applied continuously on DIN until the command is validated by the DFE-T V2.2 and the desired action has been initiated. Afterwards the command may be changed.

An indication is issued permanently by the DFE-T V2.2 on DOUT until a new indication needs to be forwarded. Because a number of states issue identical indications it is not possible to identify every state individually.

Table 13   Command / Indicate Codes

Code	LT-Mode	
	DIN	**DOUT**
0000	DR	–
0001	–	DEAC(DA)
0010	–	–
0011	LTD	– (HI)
0100	–	RSY (RSYU)
0101	SSP	–
0110	DT(TEST)	–
0111	–	UAI(RDS)
1000	AR(ARN)	AR(ARU)
1001	AR1	–
1010	AR2	–
1011	AR4	–
1100	–	AI(AIU)
1101	RES	–
1110	–	–
1111	DC(DID)	DI(DIU)

AI	Activation Indication	DI	Deactivation Indication.
AR	Activation Request	DR	Deactivation Request

AR1	Activation Request Loop 1	RES	Reset
AR2	Activation Request Loop 2	RSY	Resynchronization Indication
AR4	Activation Request Loop 4	SSP	Send-Single-Pulses
DC	Deactivation Confirmation	DT	Data Through Mode
DEAC	Deactivation Accepted	UAI	U Activation Indication
LTD	LT Disable		

3.5.10 State Machine Notation

The following state diagram describes all the actions/reactions resulting from any command or detected signal and resulting from the various operating modes.

The states with its inputs and outputs are interpreted as shown below:
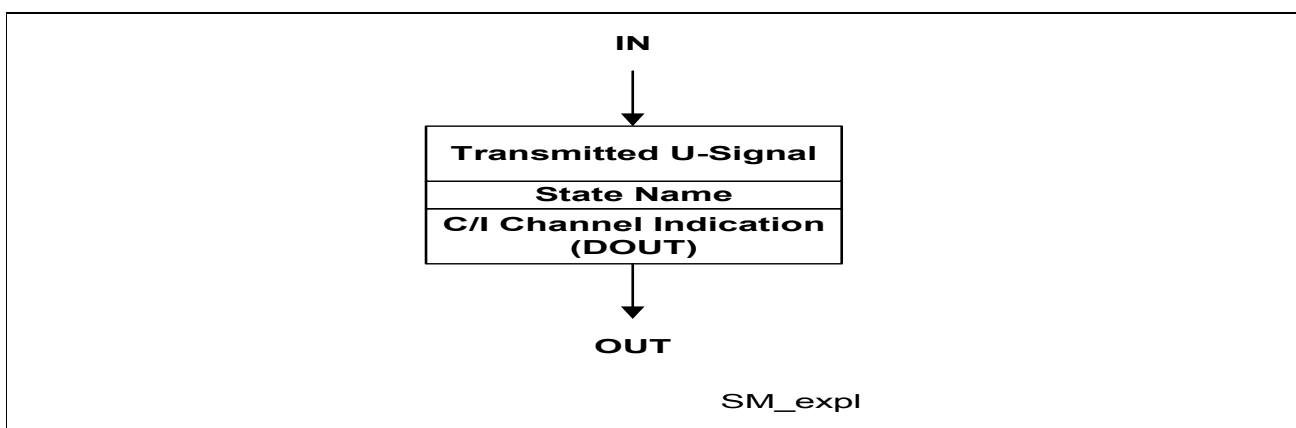
Figure 16   State Diagram Example

Each state has one or more transitions to other states. These transitions depend on certain conditions which are noted next to the transition lines. These conditions are the only possibility to leave a state. If more conditions have to be fulfilled together, they are put into parentheses with an AND operator (&). If more than one condition leads to the same transition, they are put into parentheses with an OR operator (|). The meaning of a condition may be inverted by the NOT operator (/). Only the described states and transitions exist.

At some transitions, an internal timer is started. The start of a timer is indicated by TxS ('x' is the timer number). Transitions that are caused if a timer has expired are labelled by TxE.

Some conditions lead to the same target state. To reduce the number of lines and the complexity of the figures, a state named "ANY STATE" acts on behalf of all state.

The state machine is designed to cope with all ISDN devices with IOM$^{®}$-2 standard interfaces. Undefined situations are excluded. In any case the involved devices will enter defined conditions as soon as the line is deactivated.

3.5.11 LT Mode State Diagram
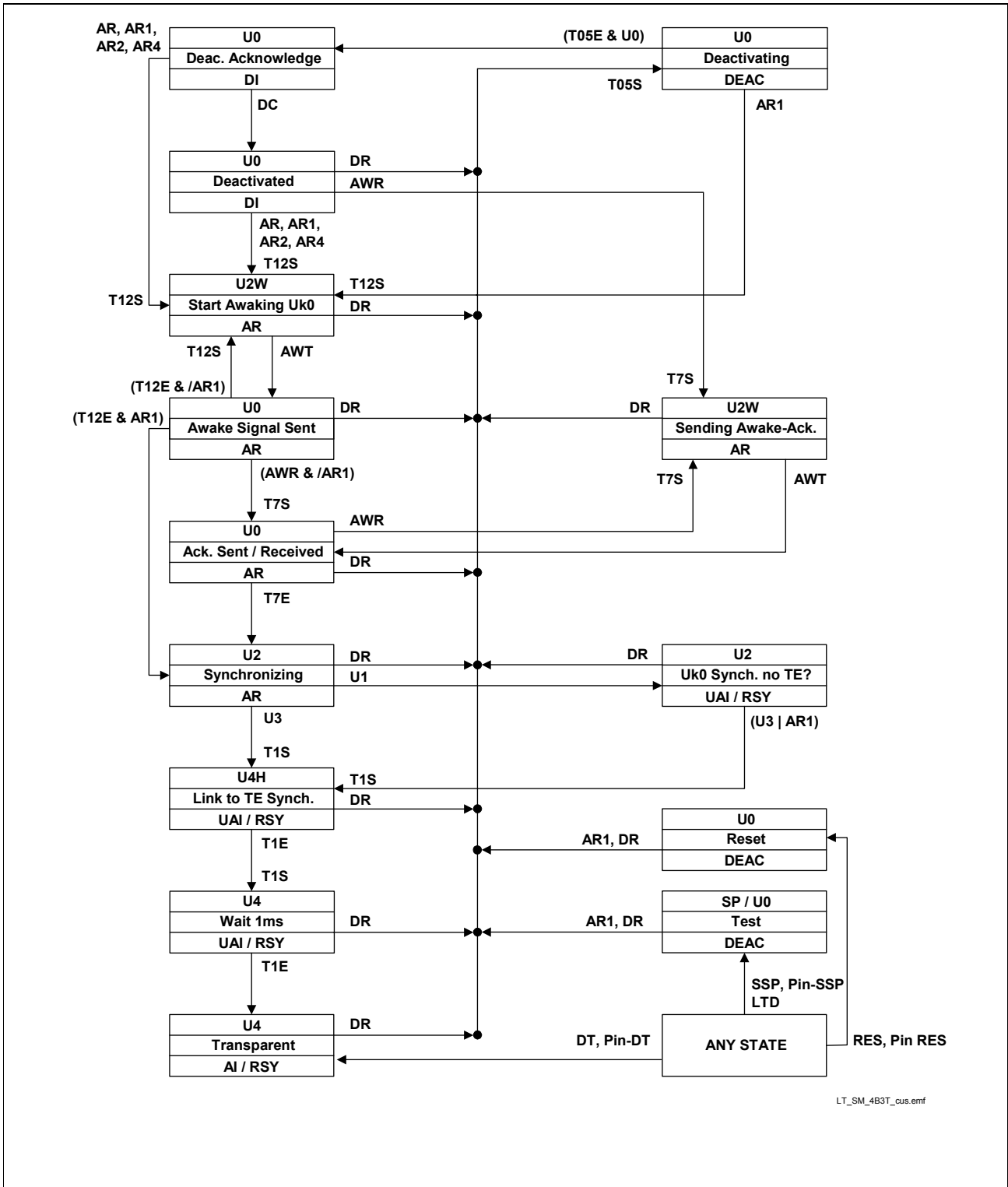
Figure 17   LT State Diagram

Table 14   Differences to the former LT-SM of the DFE-T V1.x

No.	V1.2 State/ Signal	Change in V2.2	Comment
1.	State 'Maintenance'	split into two states - Reset State - Test State	simplifies SM implementation
		transition with C/I-code 'AR1': new: from state 'Reset' or 'Test' to state 'Deactivating' old: to state 'Start Awaking Uk0': no more supported	
2.	Any State	transition condition PFOFF& / AR1 doesn't exist any more	no more support of the IEC type power controller interface
3.	State 'Maintenance'	C/I code 'HI' is omitted and no more available	
4.	State 'Power Down'	renamed to: 'Deactivated'	
5.	State 'Data Transmission'	renamed to state: 'Transparent'	
6.	Renamed C/I codes	old ->new ARN, ARU ->AR ARL->AR1 AIU->AI DA->DEAC DID->DC DIU->DI RSYU->RSY TEST->DT RDS->UAI	consistency to 2B1Q coding
7.		Timer variables introduced	Name Duration, see **Table 15**

3.5.11.1 State Machine Inputs

C/I-Commands

AR	Activation Request The U-transceiver is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal U2W.
AR1	Activation Request Local Loop-back The U-Transceiver is requested to operate an analog loop-back. An activation procedure is started. Any other C/I-channel input defined in **Table 13** causes the analog loop to be opened[1].
AR2	Activation Request Loop 2 in the NT The U-Transceiver is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal U2W. The loop 2 request is signalled via the Maintenance channel by a continuous plus polarity in the M-symbol. Any other C/I-channel input than AR2 (and AR4, see below) resets the M-symbol to zero.
AR4	Activation Request Loop 4 in the Repeater The U-Transceiver is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal U2W. The loop 4 request is signalled via the Maintenance channel by a series of alternating plus and zero polarity in the M-symbol. Any other C/I-channel input than AR4 (and AR2, see above) resets the M-symbol to zero.
DC	Deactivation Confirmation DC informs the U-transceiver that the upstream unit is also deactivated. The U-transceiver is now ready to receive awake signals. Upon DC state Deactivated is entered, where the U-transceiver allows to turn off the clocks.
DR	Deactivation Request The U-transceiver is requested to start a deactivation procedure.
DT	Data Through Test Mode Unconditional command is used for test purposes only and forces the U-transceiver to transit to the transparent state and to issue U4 independent of the wake-up protocol. A far-end transceiver needs not to be connected. In case a far-end transceiver is present it is assumed to be in the same condition.
LTD	LT Disable This unconditional command forces the U-transceiver to state Test, where it transmits info U0. No further action is initiated.

RES   Reset
            Unconditional command which resets the functions related to the channel;
            no line signal (signal U0) will be sent out.

SSP   Send Single Pulses
            Unconditional command which requests the transmission of single pulses
            with a period of 1 ms.

[1] Undefined C/I-code intputs may not open the analog loopback.

Pins

$\overline{\text{RES}}$ Pin-Reset
            A HW reset was applied and released again. Pin reset impacts all line ports
            while the SW selection impacts only the chosen line. As long as pin $\overline{\text{RES}}$ is
            low, the issued C/I-code is DI instead of DEAC for all channels. After putting
            $\overline{\text{RES}}$ to high the C/I-codes change to DEAC.

SSP   Pin-Send Single Pulses
            Corresponds to C/I code 'SSP' besides the fact that the HW selection
            impacts all line ports while the SW selection impacts only the chosen line.
            C/I-message DEAC will be issued.

U-Interface Events

U0   U0 detected
            U0 is recognized after one complete frame with continuous zero level.

U1   U1 detected
            The U-transceiver detects U1 if continuous binary '0' is found on the
            descrambler output for at least 8 subsequent U-frames. U1 is detected after
            8 to 9 ms.

U3   U3 detected
            The U-transceiver detects U3 if continuous binary '1' is found on the
            descrambler output for at least 8 subsequent U-frames. U3 is detected after
            8 to 9 ms.

AWR   Awake signal (U1W) detected

AWT   Awake signal (U2W) has been sent out

TxE   Timer ended, the started timer has expired

Timers

The start of timers is indicated by TxS, the expiry by TxE. The following table shows which timers are used.

Table 15   Timers

Timer	Duration (ms)	Function	State
T05	0.5	C/I code recognition	Deactivated
T1	1.0	Defines duration of U4H	Link to TE Synch
		NT reaction time	Wait 1ms
T7	7.0	Supervises U1W repetition	Ack. sent / received
			Sending awake- ack.
T12	12.0	Supervises U2W repetition	Start awaking Uk0,
			Awake signal sent

3.5.11.2 State Machine Outputs

Below the signals and indications are summarized that are issued on IOM®-2 (C/I-indications) and on the U-interface (predefined U-signals).

C/I Indications

AR   Activation Request
          The AR code indicates that a start-up procedure is in progress.

AI   Activation Indication
          'AI' indicates that the whole transmission line is now synchronized and transparent from the LT to the TE or that the test loop #1 has been activated..

DEAC   Deactivation Accepted
          DEAC is issued in response to a DR-code and in the states Reset and Test.

DI   Deactivation Indication
          DI informs the upstream unit that the U-transmission line is deactivated.

RSY   Resynchronization Indication
            RSY informs that the U-transceiver is not synchronous. RSY is issued if the
            U-transceiver is in one of the fully activated states and has lost
            synchronization afterwards (transmission of U signal will not be
            interrupted).

UAI   U-Activation Indication
            The U-transceiver has detected U1 or U3 indicating that the transmission
            line between the two U-interface stations is now synchronized.

Signals on U-Interface

The signals U0, U2W, U2, U4H, U4 and SP are transmitted on the U-interface. They are
defined in detail in **Table 12 "4B3T Signal Elements" on Page 52**.

Signals on IOM-2

The Data (B+B+D) is set to all '1's in all states besides the states listed in **Table 16**.

3.5.11.3   State Description

In this section each LT state is described with its function.

The C/I-channel output and the transmitted signal elements on U are already specified
by the state diagram. Below they are only referred to, if within a state there are more than
one of them specified. In this case, the C/I-channel output and the transmitted signal
element depend on the given inputs.

Acknowledge Sent / Received

If awaking the U-transceiver has received the acknowledge signal. If being awoken the
U-transceiver has sent the acknowledge. In both cases the U-transceiver waits for a
possible repetition or time-out.

Awake Signal Sent

The U-transceiver is awaking the U-interface and waits for the acknowledge by the NT
or for the time-out (12 ms) after sending the awake signal.

Deactivation Acknowledge

In the Deactivation Acknowledge state no signal (signal U0) is transmitted on the U-
interface. The U-transceiver is ready to enter the power-down state.

Deactivating

The U-transceiver deactivates the U-interface sending U0 and waits in turn for signal U0 to enter the 'Deactivated' state. Timer T05 ensures that the C/I code DEAC is recognized by the exchange.

Deactivated

On the receipt of 'DC' in the C/I channel the U-transceiver may enter the power-down state. In power-down mode all power consuming parts of the device which are not required for the wake-up detection are switched off.
The U-transceiver waits either for an activation request (AR, AR1, AR2, AR4) from the exchange or for a wake-up signal U1W from the NT.

Link to TE Synchron

The whole transmission system from the LT to the TE is now synchronized in both directions of transmission. Signal U4H is sent until the expiry of timer T1. U4H requires the NT to establish a transparent link to the TE.

If synchronization has been lost the U-transceiver issues RSY on the C/I-channel until it has resynchronized again.

Reset

The Reset state is entered by the unconditional command RES or pin-$\overline{\text{RES}}$. All stored coefficients are erased. The U-transceiver leaves the Reset state if pin-$\overline{\text{RES}}$ is set inactive ('1') and the C/I code DR or AR1 is applied. The U-transceiver does not react on the receipt of a wake-up signal.

Synchronizing

After the awake procedure, the U-transceiver trains its receiver coefficients until it is able to detect the signals U1 or U3.

Sending Awake-Acknowledge

On the receipt of the awake signal U1W the U-transceiver responds with the transmission of U2W.

Start Awaking Uk0

On the receipt of AR, AR1, AR2 or AR4 in the C/I-channel the U-transceiver is sending the awake signal U2W.

Uk0 Synch. no TE?

After the recognition of U1 the U-interface is synchronized in both directions. That is 1152 subsequent bits have been transferred and received without any bit error. In case of an analog loop the U-transceiver leaves this state again immediately.

If in 64 subsequent U-frames the Barker-code can not be detected at the expected position, the U-transceiver issues RSY on the C/I-channel until it has resynchronized. The criteria for resynchronization is that the Barker-code has been detected at the same position in 4 subsequent frames.

Test

Test mode is entered by the unconditional command LTD, SSP or pin-SSP. The Test state is left if pin SSP is set inactive ('0') and the C/I code DR or AR1 is applied. The test signal SSP is issued as long as pin SSP is active or C/I=SSP is applied.

Transparent

The transmission line is fully activated. User data can be exchanged by U4/U5. Transparent state may also be entered in the case of a loop-back 1. The exchange is informed by C/I code AI that the transparent state has been reached.

If synchronization has been lost the U-transceiver issues RSY on the C/I-channel until it has resynchronized again.

Wait 1 ms

If the Wait 1 ms state has been reached, the U-Transceiver in the exchange waits 1 ms to ensure that the whole link is already transparent before it is indicated by C/I code AI to the exchange.

If synchronization has been lost the U-transceiver issues RSY on the C/I-channel until it has resynchronized again.

3.6 Clock Generation

The U-transceiver has to synchronize onto an externally provided PTT-master clock. A phase locked loop (PLL) is integrated in the AFE (PEF 24902) to generate the 15.36 MHz system clock. A synchronized system clock guarantees that U-interface transmission will be synchronous to the PTT-master clock.

The AFE is able to synchronize onto a 8 kHz or a 2048 kHz system clock. **Infineon recommends to feed the FSC clock input of the DFE-T V2.2 and the PLL reference clock input (pin CLOCK) of the AFE from the same clock source.** Please refer to the PEF 24902 Data Sheet for further details on the PLL.

For the connection of the AFE clock output line with the DFE-T V2.2 clock input line (CL15) please refer to **Figure 4** and **Figure 5**.

4 Operational Description

The scope of this section is to describe how the DFE-T V2.2 works and behaves in the system environment. Activation/ deactivation control procedures are exemplary given for SW programmers reference.

4.1 Reset

There are two different ways to apply a reset,

- either as a hardware reset by setting pin $\overline{RES}$ to low
- or as a software reset by applying 'C/I= RES'

Hardware Reset

A hardware reset affects all design components and takes effect immediately (asynchronous reset style). No clock signal other than the 15.36 MHz master clock shall be required for reset execution.

Software Reset

A software reset triggered by 'C/I= RES' has only effect on the addressed line port. The remaining line ports, the system interface, the relay driver/ status pins and any global functions are not affected. Note that FSC and DCL clock signal must be provided for the C/I code processing.

C/I 'RES' resets the receiver and the activation/deactivation state machine. Transmission on U is stopped (signal U0). It is an unconditional command and is therefore applicable in any state.

4.2 Power Down

Each building block of the DFE-T V2.2 is optimized with respect to power consumption and support a power down mode. See chapter **Chapter 7.6.2** for the specified max. power consumption.

The DFE-T V2.2 goes in power down mode

- if the U-transceiver is in state 'Deactivated' and no MONITOR message is pending

There are two events that awake the DFE-T V2.2 again from power down mode,

- when a wake up tone (U1W) has been detected on U
- when any of the C/I codes AR, AR1, AR2 or AR4 is applied at DIN

Regarding the **DFE-T V2.2** power down mode means that

- the DSP clock is turned off
- all other digital circuits (excluding the IOM$^®$-2 interface) go in power down mode
- no timing signals are delivered (CLS0, ... , CLS3)

- as the internal control logic of the activation/deactivation procedures is event driven power is saved as soon as one of the four lines transits in the DEACTIVATED state

Regarding a connected **AFE** power down mode means that

- no signal (signal U0) is sent on the U-interface
- only functions that are necessary to detect the wake up conditions are kept active
- transmit path, receive path and auxiliary functions of the analog line port are switched to a low power consuming mode when the power down function is activated. This implies the following:
- the ADC, the relevant output is tied to GND.
- the DAC and the output buffer; the outputs AOUTx/ BOUTx are tied to GND.
- the internal DC voltage reference is switched off.
- the range and the loop functions are deactivated.

4.3   Layer 1 Activation/ Deactivation Procedures

This chapter illustrates the interactions during activation and deactivation between the LT and NT station. An activation can be initiated by either of the two stations involved. A deactivation procedure can be initiated only by the exchange. The status of a transmission line is classified by one of the seven activation/deactivation states (also referred to by number in the activation/ deactivation procedures on the following sides):

1. **Activation** States:
    1.1 **Line awake**
        Each individual line is being awoken, but is not yet synchronized, data transmission is not yet possible
    1.2 **Synchronization downstream**
        Synchronization is always done downstream first, the whole line has to synchronize on the exchange
    1.3 **Synchronization upstream**
        Because the delay differs from line to line, bit synchronization is necessary in the LT
    1.4 **Synchronized**
        All layer-1 units of the link are told by the exchange that synchronization has been finished

2. **Transparent** State:
    In the activated state, the user data is transmitted from exchange to TE and vice versa.

3. **Deactivation** States:
    Deactivation is done in two steps on each individual line separately.
    3.1 Deactivation request downstream
    3.2 Deactivation acknowledge upstream

The transmission link is totally deactivated thereafter.

The exchange of control information is partially state oriented on the U-interface. Some signal elements are given as long as no other information has to be transferred, other signal elements have distinct durations.

4.3.1   Complete Activation Initiated by Exchange

.
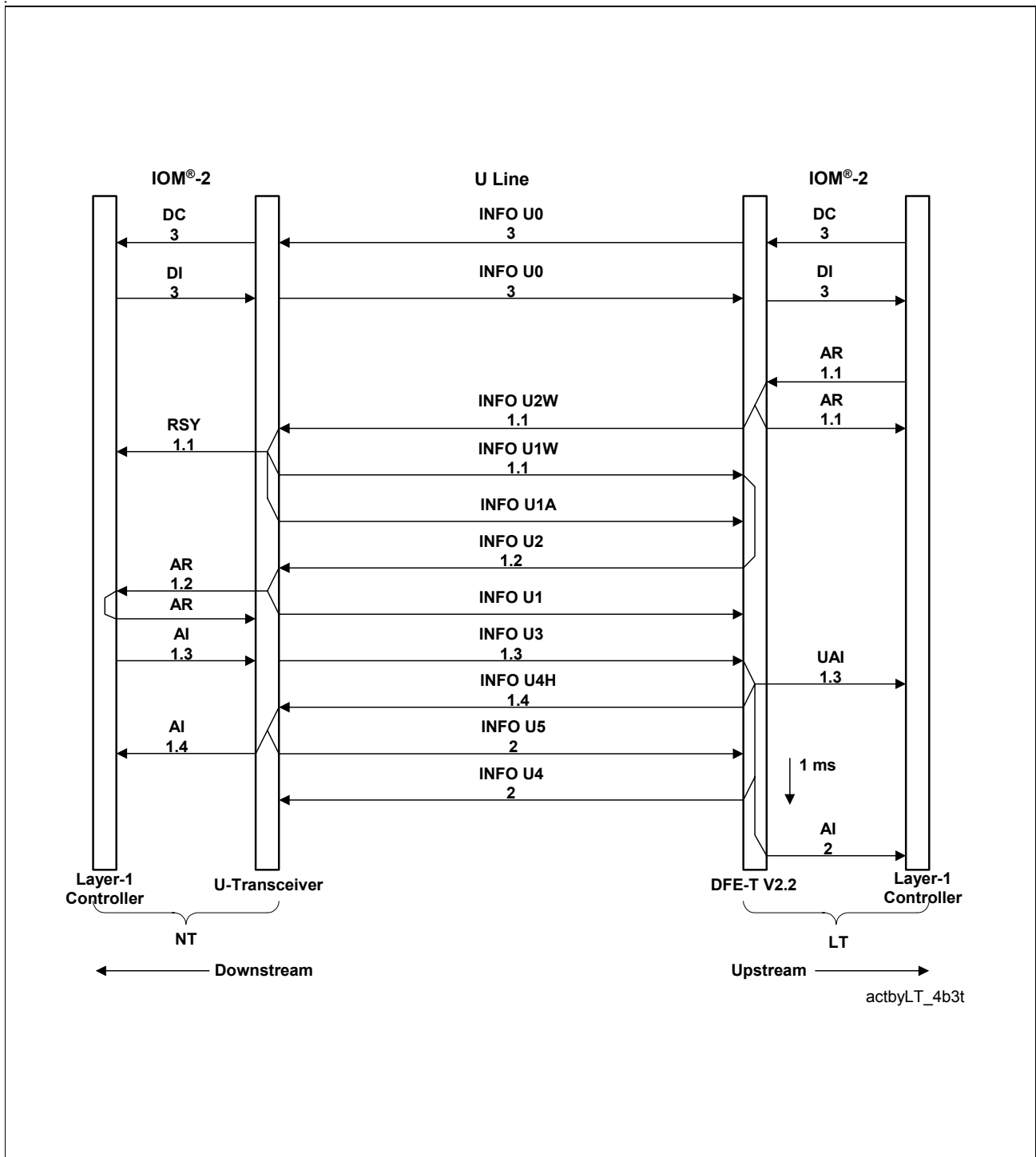
Figure 18   Activation Initiated by Exchange

4.3.2 Complete Activation Initiated by TE
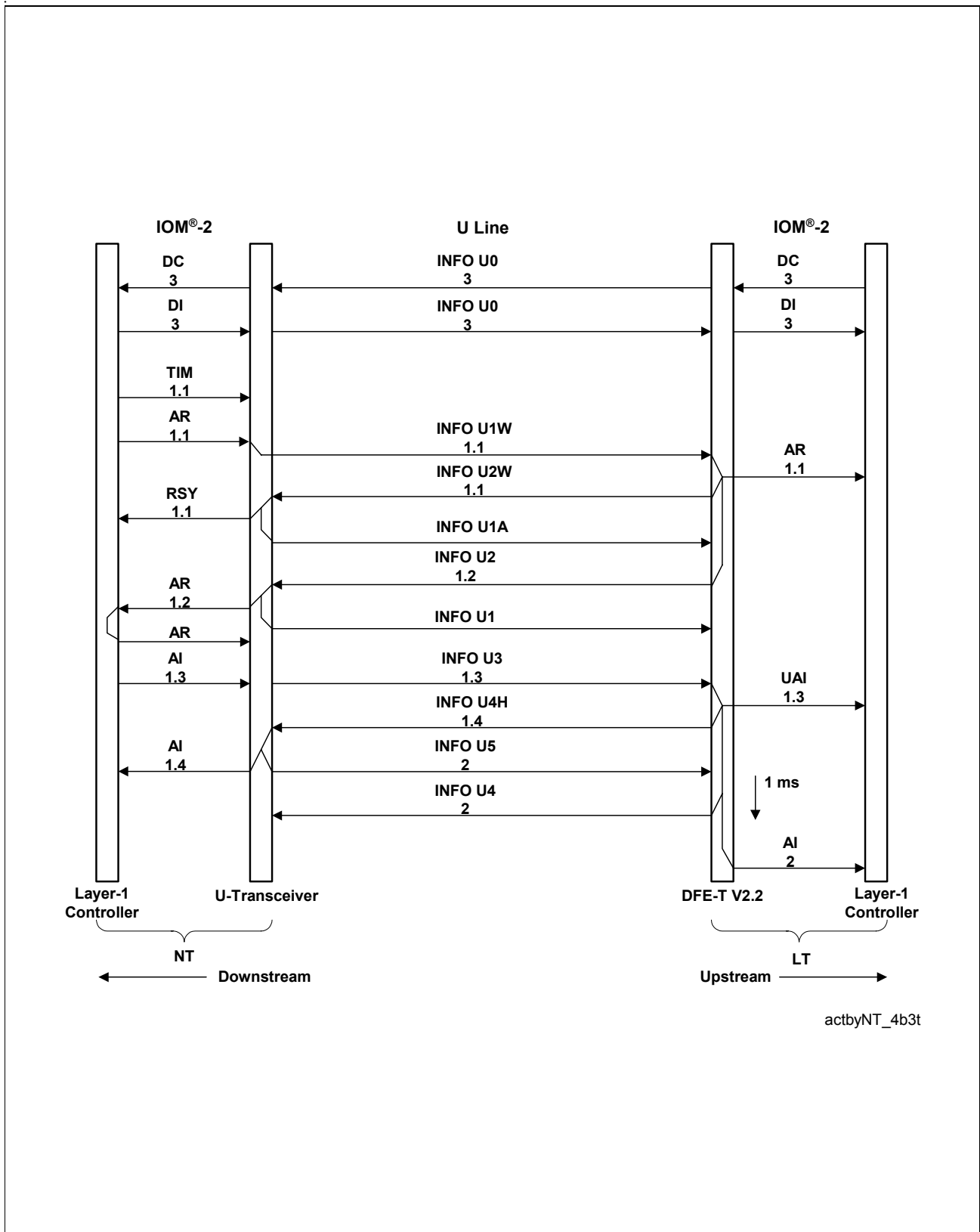
Figure 19   Activation Initiated by TE

4.3.3   Complete Activation Initiated by Exchange with Repeater
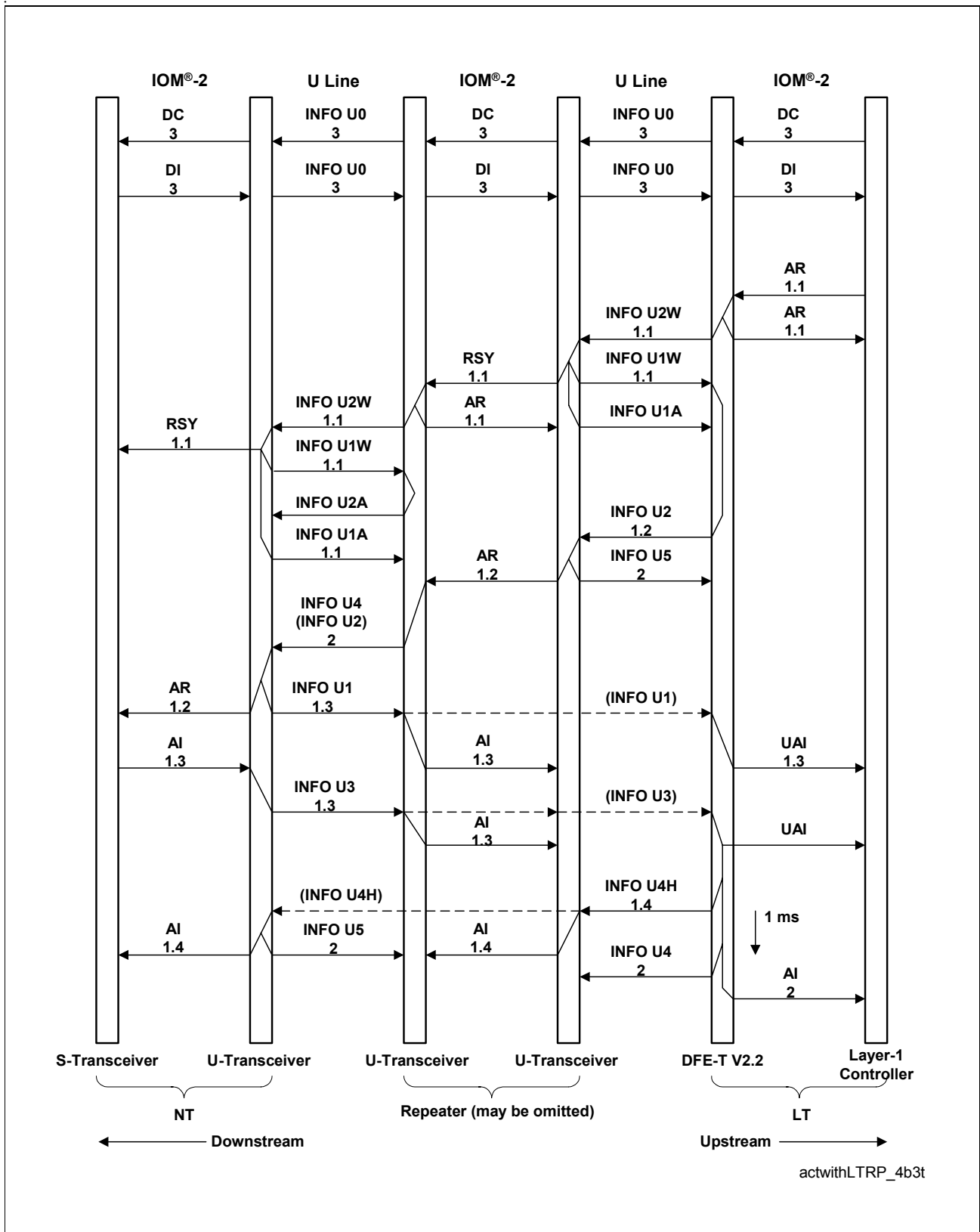
Figure 20   Activation with Repeater Initiated by LT

4.3.4 Complete Activation Initiated by Terminal with Repeater
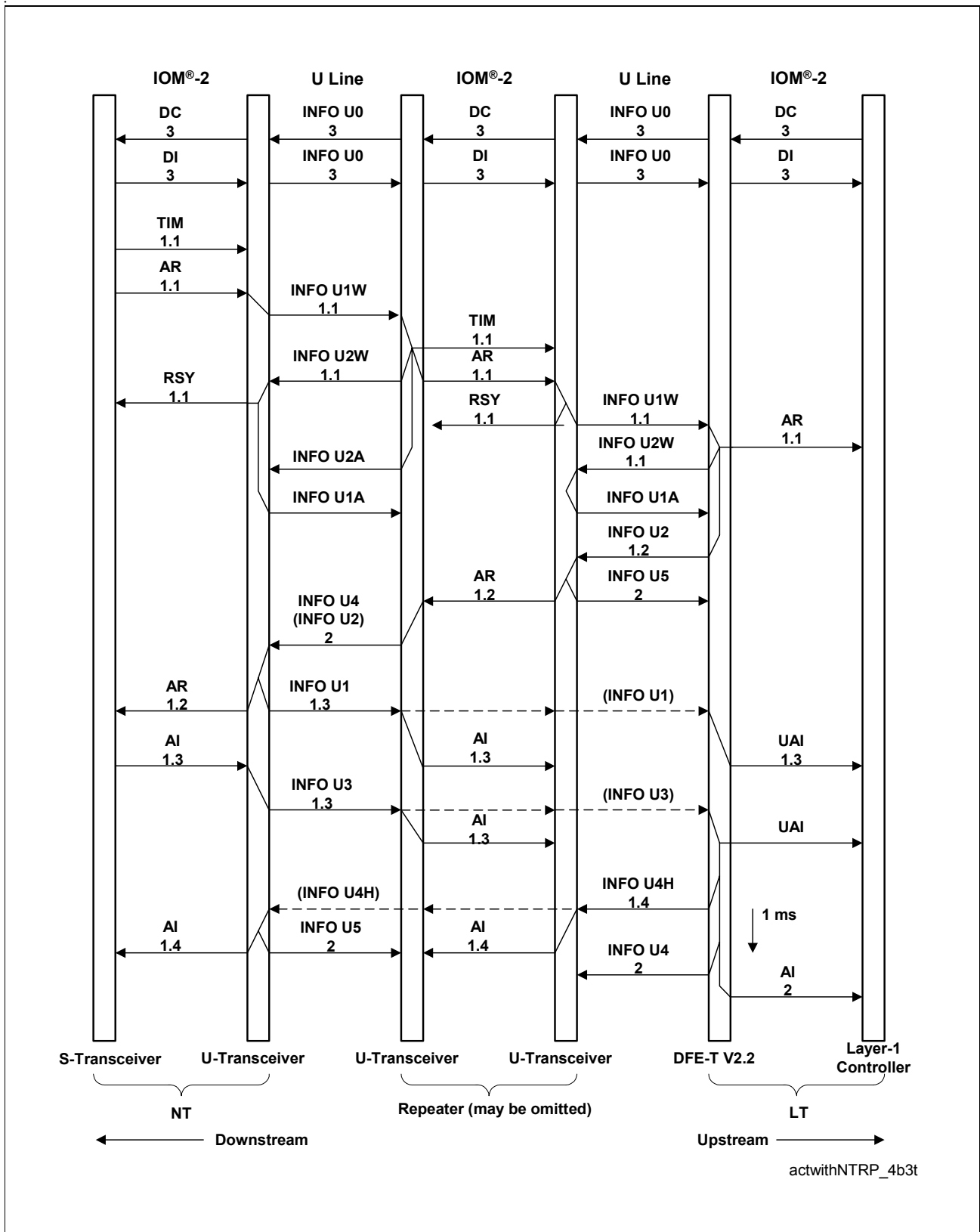
Figure 21   Activation with Repeater Initiated by TE

4.3.5 Deactivation
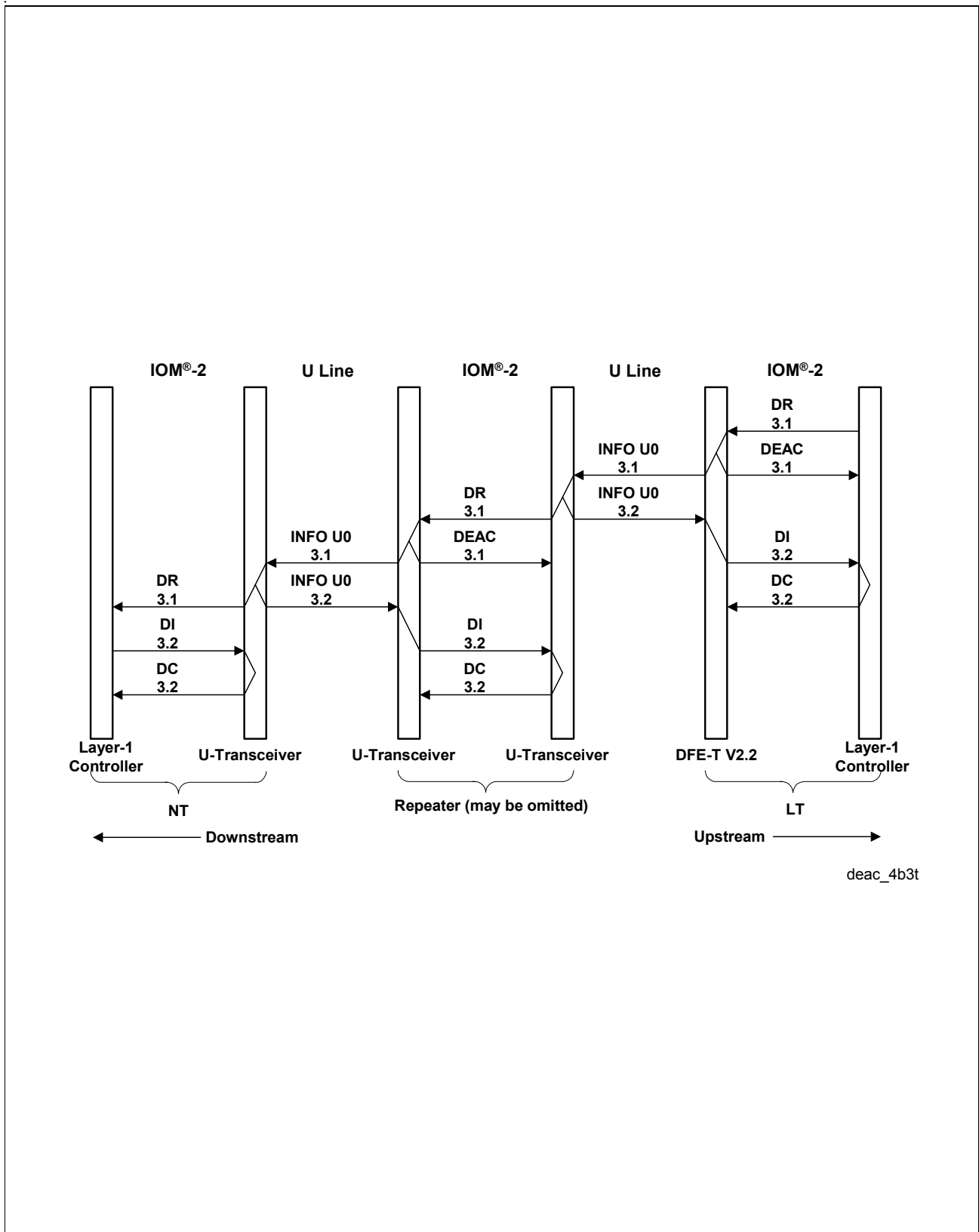
Figure 22   Deactivation (Always Initiated by the Exchange)

4.3.6 Activation of Loop#1
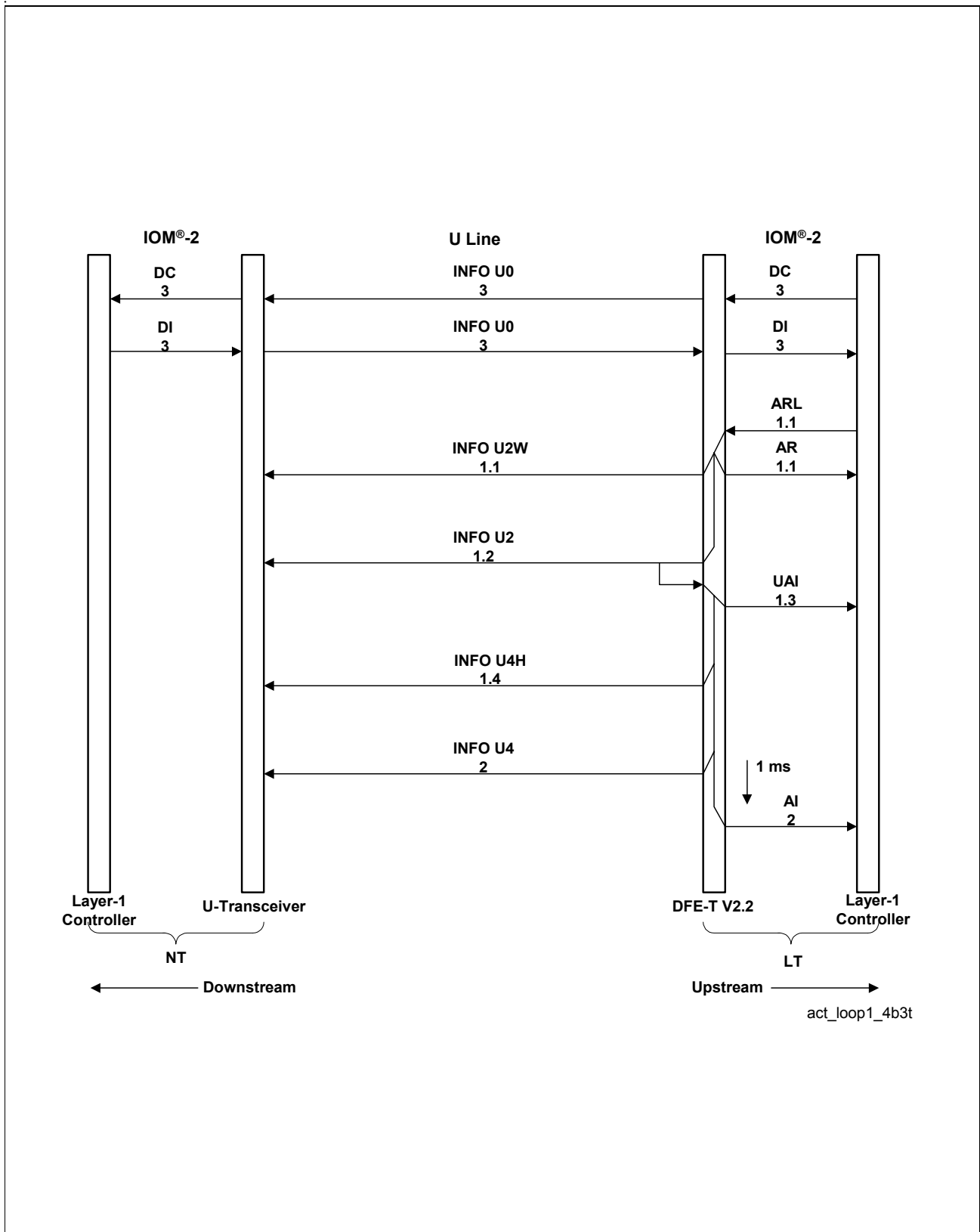
Figure 23   Activation of Loop#1

4.3.7   Activation of Loop#4
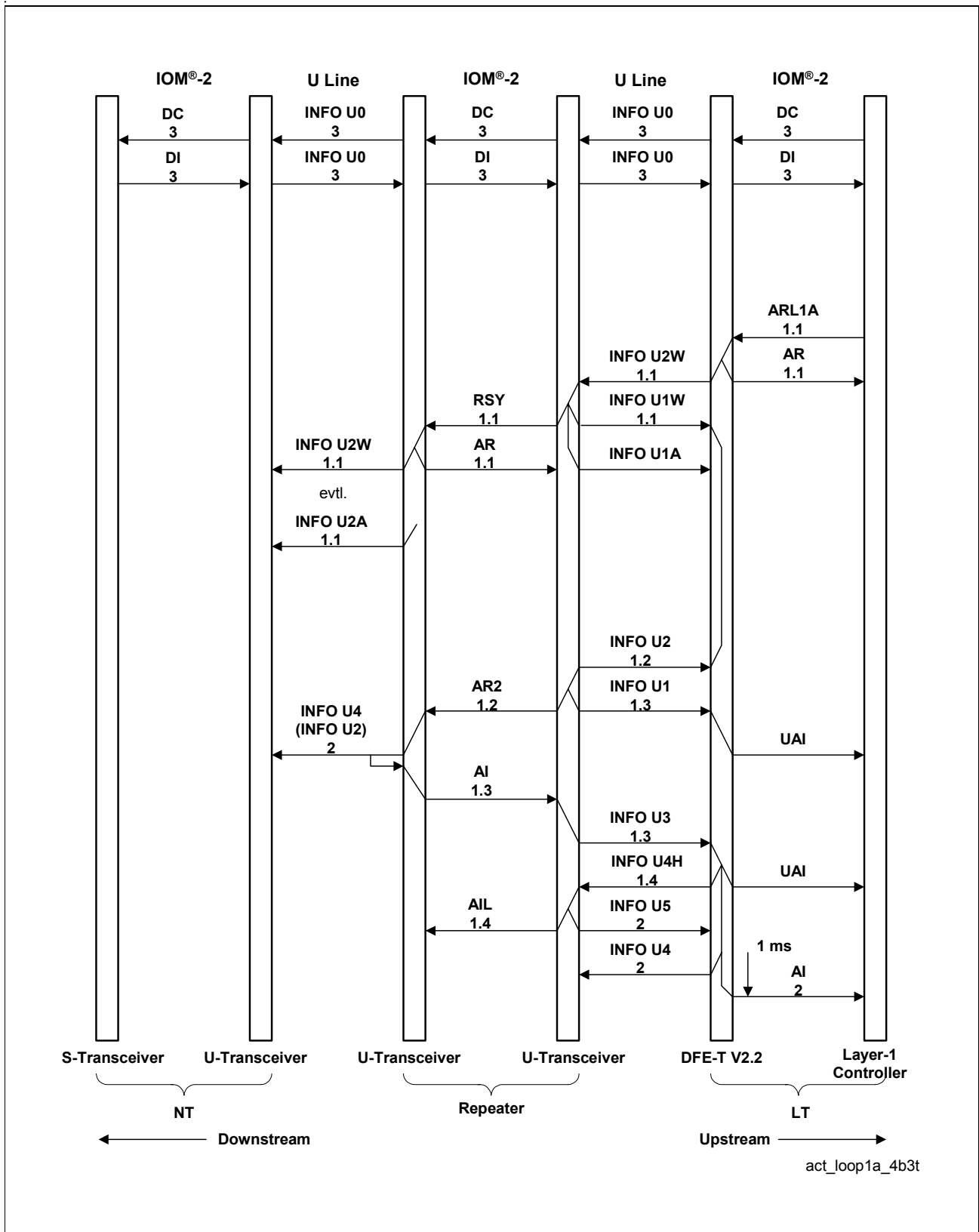
Figure 24   Activation of Loop#1A (Repeater)

4.3.8 Activation of Loop#2
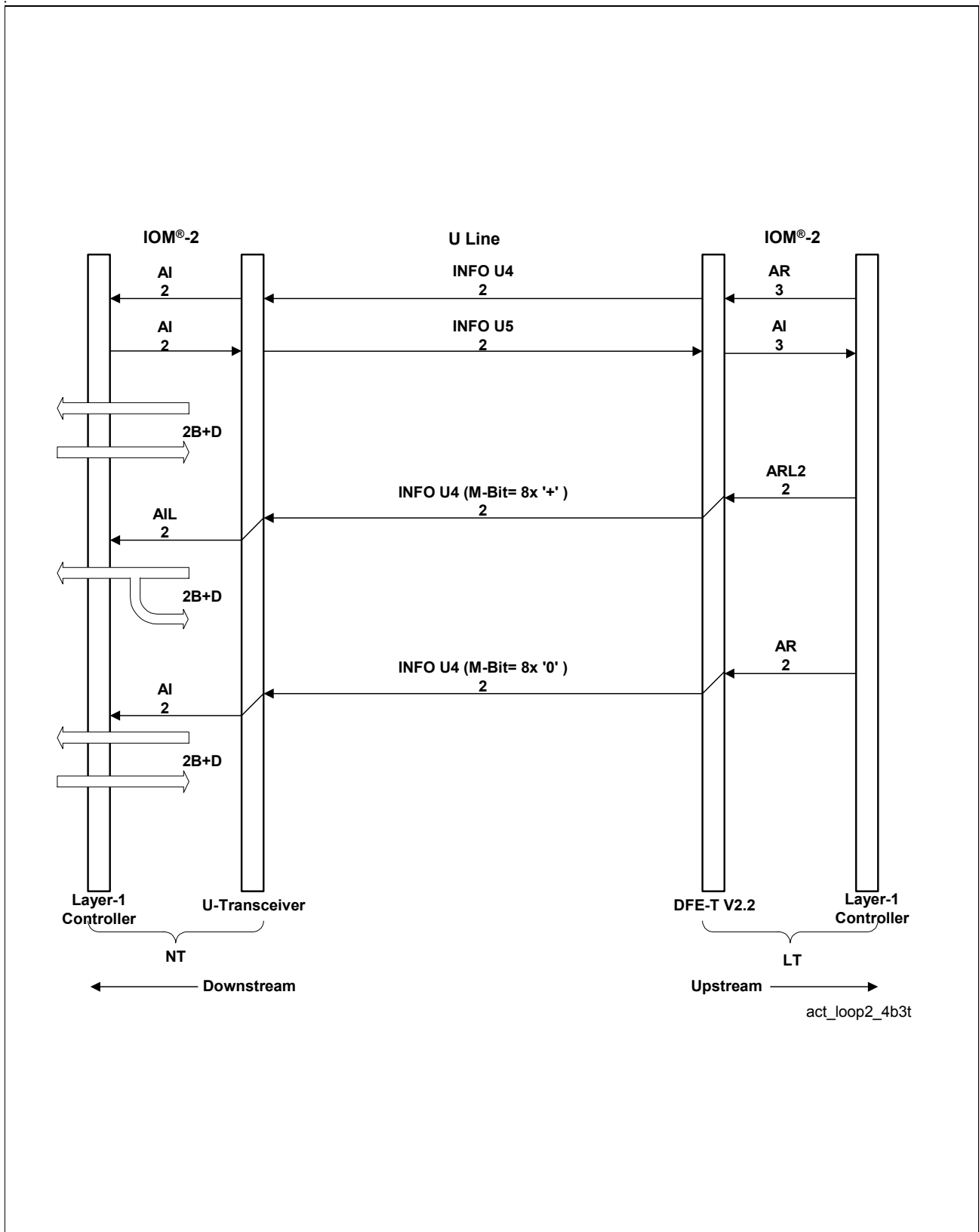
Figure 25   Activation of Loop#2

4.4 Maintenance and Test Functions

This chapter summarizes all features provided by the U-transceiver to support maintenance functions and system measurements. They are classified into three main groups:

– maintenance functions to close and open test loopbacks
– features facilitating the recognition of transmission errors
– test modes required for system measurements

The next four sections describe how these maintenance functions are used in applications.

4.4.1 Test Loopbacks

Four different loopbacks are defined for maintenance purposes and in order to facilitate the location of defect systems. The position of each loopback is illustrated in **Figure 26**. Remote control by the exchange is featured. When a test loop is closed all channels (B1 + B2 + D) are looped back and data from the other end of the line is ignored. There are no separate loops for single channels.
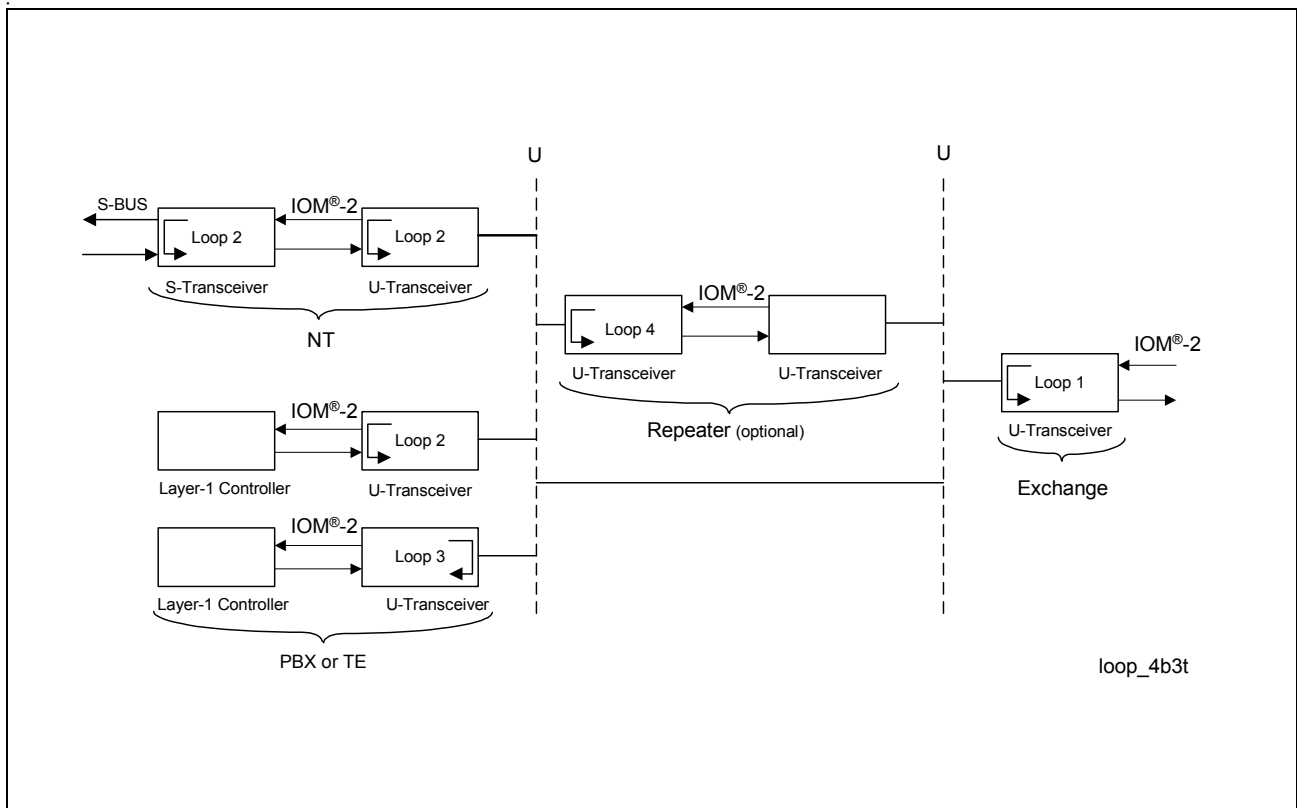
Figure 26   Test Loopbacks

All test loops are transparent loops. The line signal is still transmitted although the analog loop is closed. Nevertheless the NT receives this signal and synchronizes on it. The NT can not distinguish between line signals sent from the LT during loop 1 or loop 4 and signals sent during normal operation. Loopback no.1 is closed by the DFE-T V2.2 itself, whereas loopback no 4 and no.2 are remote controlled by C/I code 'AR4' and 'AR2' and are closed in the repeater or in the NT, respectively. Loopback no.3 is not supported since the DFE-T V2.2 operates only in LT mode.

4.4.1.1 Analog Loopback (No.1)

The analog loop no.1 is closed in the DFE-T V2.2 as close to the U-interface as possible. The signal from the line driver is fed back directly to the input. It is like a short-circuit between the pins AOUT and AIN as well as between BOUT and BIN. The input signal

from the hybrid is ignored in this mode. The analog loop mode is controlled via the IOM®-2 C/I-channel code 'AR1'.

To request a LT-repeater to close the analog loop no.4, C/I code 'AR4' must be applied to the DFE-T V2.2. It will send in turn alternating plus and zero polarity within 8 subsequent frames in the M-channel (+ 0 + 0 + 0 + 0 ...).

4.4.1.2   Loopback No.2

Loopback no. 2 is controlled by the exchange. It is transparent which means that all bits that are looped back are also passed on to the S-bus. The DFE-T V2.2 features the remote control of loop no.2 via its C/I channel. C/I code 'AR2' requests the NT to close the loop, 'AR' or 'DR' requests the NT to open the loop again.

The DFE-T V2.2 translates the received C/I codes into the following pattern sequence in the M-channel of the U-interface:

- continuous '+' polarity
  The NT closes loopback no.2 after 8 consecutive pulses with plus polarity has been received in the M-channel (+ + + + + + + + ...).
- continuous '0' polarity
  The NT clears loopback no.2 after 8 consecutive zeros has been received in the M-channel (0 0 0 0 0 0 0 0 ...) or on a deactivation request.

During normal transmission without loops, the M-symbol is set to zero.

The loopback comprises both B-channels and the D-channel. It is closed in the NT as close to the S-transceiver as possible.

4.4.1.3   Available Loopbacks by Register Map

Besides the standardized remote loopbacks the DFE-T V2.2 features additional local loopbacks for enhanced test and debugging facilities. The loopbacks that are additionally available with the internal LOOP register are shown in **Figure 27**.They are closed in the DFE-T V2.2 itself.

By the LOOP register it can be configured whether the digital looback is closed only for the B1 and/or B2 or for all ISDN-BA channels and whether the loopback is closed towards the IOM®-2 interface or towards the U-Interface.

The bit TRANS in the LOOP register allows for selection of transparent or non-transparent loopback mode. In transparent mode the data is both passed on and looped back. In non-transparent mode the data is not forwarded but substituted by 1 s (idle code).

Note: The digital framer/deframer loopback (DLB) is always transparent.

Besides the loopbacks in the system interface a further digital loopback, the Framer/Deframer loopback is featured. It allows to test all digital functions of the 4B3T U-transceiver besides the signal processing blocks. However, an activation procedure is

not possible by closing the Framer/Deframer Loopback. Therefore, before loop DLB may be closed, the DFE-T V2.2 must be in a transparent state, e.g. by applying C/I-command 'Data Through DT'. If DLB is set to '1' in state 'Deactivated', then a subsequent activation fails.

Note: Block errors will be noticed, while DLB is active and a remote loop back (C/I=AR2 or AR4) is commanded. Bits LB1, LB2, LBBD and U/IOM should be set to '0' before closing the Digital Loopback.Otherwise, contradictory commands may conflict with each other.
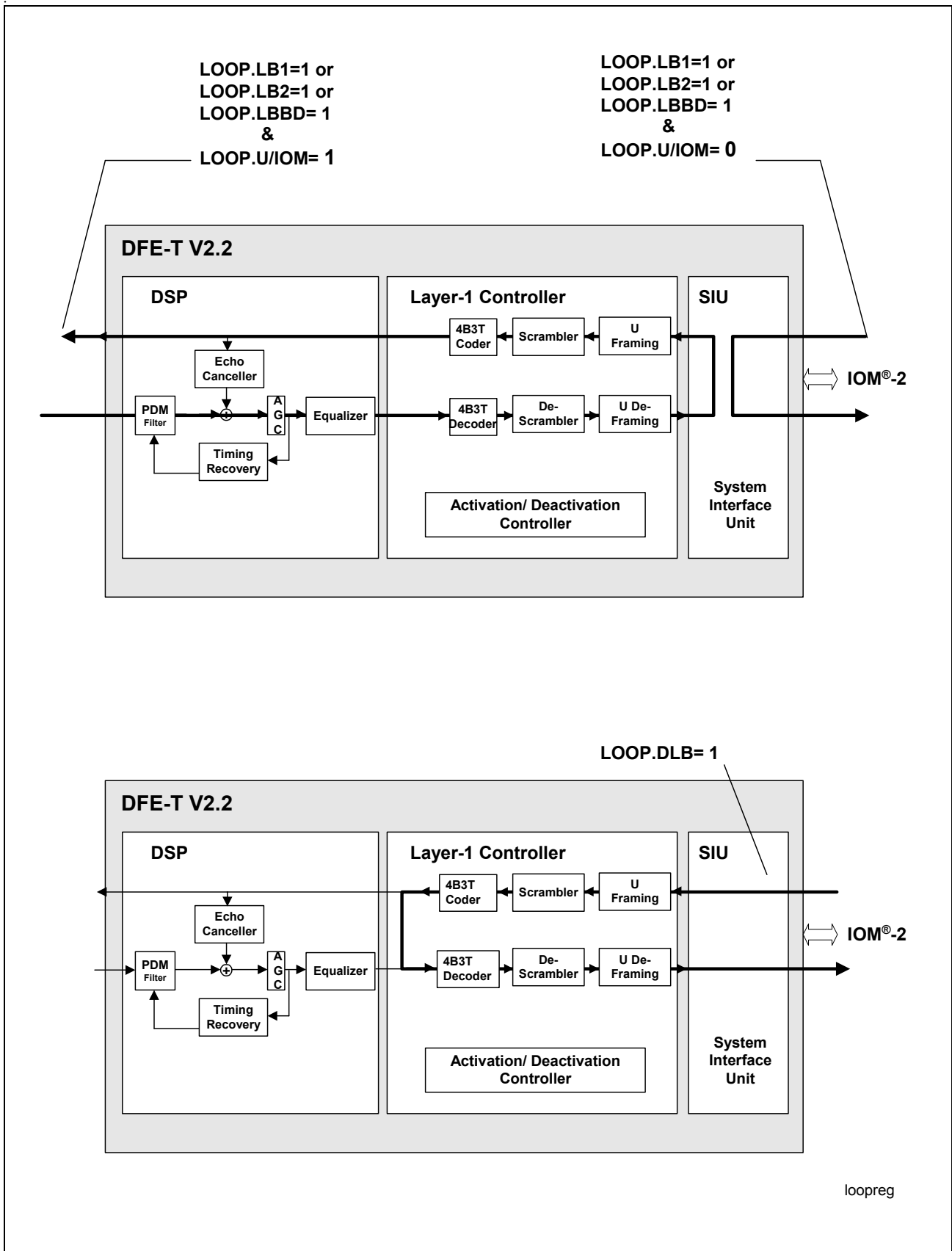
Figure 27   Loopbacks Featured by Register LOOP

4.4.2   Block Error Counter (RDS Error Counter)

The DFE-T V2.2 provides a block error counter per channel. This feature allows monitoring the transmission quality on the U-interface.

On the NT side a block error is given, if a U-frame with at least one code violation has been detected (near-end block error). In the following frame the NT transmits a positive M-symbol upstream.

On the LT side a block error is given, if a U-frame with at least one code violation has been detected (near-end block error) or a positive M-symbol has been received from the NT (far-end block error).

The current status of the block error counter can be retrieved by the IOM-2 interface. When the block error counter is read (via MON-8 command RDS or MON-12 read access to register RDS), it is automatically reset. The counter is enabled in all states listed in **Table 16** and reset in all other states. The counter is saturated at its maximum value (255).

Table 16   Active States

U_{k0} Synch. no TE ?
Link to TE Synch.
Wait 1ms
Transparent

Note that every frame with a detected code violation causes about 10 to 20 binary bit errors on average. So a bit error rate of 10^{-7} in both directions is equivalent to 2 detected frame errors within 1000 s in the LT (1 frame error detected in the NT and transmitted via M-symbol).

4.4.3   Bit Error Rate Counter

For bit error rate monitoring the DFE-T V2.2 features an 16-bit Bit Error Rate counter (BERC) per line. The function is channel selective. The measurement is performed for the B1, B2 and the D channel. Prerequisite is that loop #2 of the addressed line port has been closed before on the NT side via the M-channel.

Operation:

- The respective loopback command has to be transmitted to the NT.
- The system sets the respective channel to 'all zeros'.
- The respective lineport is addressed by setting the LP_SEL register.
- The BERC counter is reset to '0000' by reading the low significant BERC register.
- The BERC counter can be started after some time (full round trip delay) by selecting the channel (s) to be checked in bits TEST.BER.

- The BERC is stopped by setting TEST.BER to '00'.
- The number of bit errors (received '1's) can be read in register BERC.
- The system can enable normal data transmission again.

4.4.4 System Measurements

The DFE-T V2.2 features dedicated test modes to enable and ease system measurements. How these test modes can be used to conduct the most frequently needed system measurements is described in the following sections.

4.4.4.1 Send Single Pulses Test Mode (SSP)

In the send-single-pulses test mode, the U-transceiver transmits on the U-interface $+1$ pulses spaced by 1 ms. Two options exist for selecting the "Send-Single-Pulses" (SSP) mode:

– hardware selection: Pin-SSP= '1' (see **Table 3**)[1]
– software selection: C/I code= SSP (0101_B)

Both methods are fully equivalent besides the fact that the HW selection impacts all line ports while the SW selection impacts only the chosen line. The SSP-test mode is required for pulse mask measurements.

4.4.4.2 Data Through Mode (DT)

When selecting the data-through test mode the DFE-T V2.2 is forced directly into the "Transparent" state. This is possible from any state in the state diagram.

Note: Data-Through is a pure test mode. It is not suited to replace the activation/ deactivation procedures for normal operation, which are described in **Chapter 4.3**.

The Data-Through option (DT) provides the possibility to transmit a standard scrambled U-signal even if no U-interface wake-up protocol is possible. This feature is of interest if no counter station can be connected to supply the wake-up protocol signals. As with the SSP-mode, two options are available.

– hardware selection: Pin-DT= '1' (see **Table 3**)[1]
– software selection: C/I code= DT (0110_B)

Note that the hardware selection offers the option to initiate further actions via C/I-code (e.g. simultaneous stimulation of an analog loop-back by C/I 'AR1').

The DT-mode is required for power spectral density and total power measurements.

---

[1] The digital interface has to be active, before pin-SSP / pin-DT become effective (see **Page 43**)

4.4.4.3 Reset Mode

In the reset mode the DFE-T V2.2 does not transmit any signals. The chip is in the "Reset" state. All echo canceller and equalizer coefficients are reset. As can be seen from the state diagram, no activation is possible if the device is in the "Reset" state.

For measurements two methods are recommended in order to transfer the U-transceiver into the master-reset mode:

– hardware selection: Pin-$\overline{\text{RES}}$= '0' (see **Table 3**)
– software selection: C/I-code= RES (0001_B)

The reset test mode is used for the return-loss measurements.

4.4.4.4 Pulse Mask Measurement

– Pulse mask is defined in FTZ Guideline 1TR 220 and ETSI TS 102 080
– U-interface has to be terminated with 150 Ω
– U-transceiver is in "Send-Single-Pulses" mode (C/I = 'SSP' or Pin-SSP = '1')
– Measurements are done using an oscilloscope

4.4.4.5 Power Spectral-Density Measurement

– PSD is defined in FTZ Guideline 1TR 220 and ETSI TS 102 080
– U-interface has to be terminated with 150 Ω
– U-transceiver is in "Data-Through" mode (C/I = 'DT' or Pin-DT= '1')
– For measurements a spectrum analyzer is employed

4.4.4.6 Return-Loss Measurement

– Return loss is defined in FTZ Guideline 1TR 220 and ETSI TS 102 080
– U-transceiver is in "Reset" state (C/I = 'RES' or Pin-$\overline{\text{RES}}$= '0')
– Measure complex impedance "Z" from 5 kHz – 100 kHz
– Calculate return loss with formula:
  RL(dB) = 20log (abs((Z + 150) / (Z −150)))

4.4.4.7 Quiet Mode Measurement

– Quiet mode is defined in FTZ Guideline 1TR 220 and ETSI TS 102 080
– U-transceiver is in the "Reset" state (C/I = 'RES' or Pin-$\overline{\text{RES}}$= '0')
– Trigger and exit criteria have to be realized externally

4.4.4.8 Insertion Loss Measurement

– Insertion loss is defined in FTZ Guideline 1TR 220 and ETSI TS 102 080
– U-transceiver is in "Data-Through" mode (C/I = 'DT' or Pin-DT= '1')
– Trigger and exit criteria have to be realized externally

4.4.5 Boundary Scan

The DFE-T V2.2 provides a boundary scan support for a cost effective board testing. It consists of:

- Boundary scan according to IEEE 1149.1 specification
- Test Access Port controller (TAP)
- Five dedicated pins (TCK, TMS, TDI, TDO, $\overline{\text{TRST}}$)
- Pins $\overline{\text{TRST}}$, TDI and TMS are provided with an internal pullup resistor
- One 32-bit IDCODE register
- Pin $\overline{\text{TRST}}$ tied to low resets the Boundary Scan TAP Controller (recommended setting for normal operation if the Boundary Scan logic is not used)
- Instructions CLAMP and HIGHZ were added, instruction SSP was removed in V2.2

Boundary Scan

All pins except the power supply pins, the "Not Connected" pins and the pins TDI, TDO, TCK, TMS, and $\overline{\text{TRST}}$ are included in the boundary scan chain. Depending on the pin functionality one, two or three boundary scan cells are provided.

Note: Pin 16 (former MTO) and pin 49 (former TP3) are included in the Boundary Scan despite they are N.C. (not connected) in the pin list.

Table 17   Boundary Scan Cells.

Pin Type	Number of Boundary Scan Cells	Usage
Input	1	input
Output	2	output, enable
I/O	3	input, output, enable

When the TAP controller is in the appropriate mode data is shifted into or out of the boundary scan via the pins TDI/TDO using the 6.25 MHz clock on pin TCK.

The pins are included in the following sequence in the boundary scan chain:

Boundary Scan Number TDI —>	Pin Number	Pin Name	Type	Number of Scan Cells
1.	62	DT	I	1
2.	61	CLS3	I/O	3
3.	60	$\overline{\text{RES}}$[1]	I	1
4.	56	SSP	I	1

Boundary Scan Number TDI —>	Pin Number	Pin Name	Type	Number of Scan Cells
5.	55	SLOT0	I	1

In V2.2 pin 53 is not provided with a BScan cell (N.C.)

Boundary Scan Number TDI —>	Pin Number	Pin Name	Type	Number of Scan Cells
6.	52	CLS2	I/O	3
7.	51	D3D	I/O	3
8.	50	D2D	I/O	3
9.	49	N.C. (former TP3)	I	1
10.	48	D1D	I/O	3
11.	47	D0D	I/O	3
12.	46	D3C	I/O	3
13.	45	SLOT1	I	1
14.	44	D2C	I/O	3
15.	43	D1C	I/O	3
16.	42	D0C	I/O	3
17.	40	D3B	I/O	3
18.	39	D2B	I/O	3
19.	37	D1B	I/O	3
20.	35	D0B	I/O	3
21.	34	D3A	I/O	3
22.	33	D2A	I/O	3
23.	32	PUP	I	1
24.	31	D1A	I/O	3
25.	30	D0A	I/O	3
26.	29	CLS0	I/O	3
27.	28	ST00	I	1
28.	27	ST01	I	1
29.	26	ST10	I	1
30.	24	ST11	I	1
31.	23	ST20	I/O	3

Boundary Scan Number TDI —>	Pin Number	Pin Name	Type	Number of Scan Cells
32.	21	ST21	I/O	3
33.	20	CLS1	I/O	3
34.	19	ST30	I/O	3
35.	18	ST31	I/O	3
36.	17	SDX	I/O	3
37.	16	N.C. (former MTO)	I	1
38.	15	DOUT	I/O	3
39.	14	DIN	I	1
40.	13	FSC	I	1
41.	12	DCL	I	1
42.	11	PDM0	I	1
43.	10	PDM1	I	1
44.	8	PDM2	I	1
45.	7	PDM3	I	1
46.	5	SDR	I	1
47.	4	CL15	I	1

[1] In the BDSL file, pin 60 is named RESQ.

TAP Controller

The *Test Access Port* (TAP) controller implements the state machine defined in the JTAG standard IEEE 1149.1. Transitions on the pin TMS cause the TAP controller to perform a state change. Before operation the TAP controller has to be reset by $\overline{\text{TRST}}$. According to the IEEE 1149 standard 7 instructions are executable. The instructions 'CLAMP' and 'HIGHZ' were added. Instruction 'SSP' is no more supported since its function is identical to that of the SSP pin.

Table 18   TAP Controller Instructions

Code	Instruction	Function
0000	EXTEST	External testing
0001	INTEST	Internal testing
0010	SAMPLE/PRELOAD	Snap-shot testing

Code	Instruction	Function
0011	IDCODE	Reading ID code
0100	CLAMP	Reading outputs
0101	HIGHZ	Z-State of all boundary scan output pins
1111	BYPASS	Bypass operation

EXTEST is used to examine the board interconnections.

When the TAP controller is in the state "update DR", all output pins are updated with the falling edge of TCK. When it has entered state "capture DR" the levels of all input pins are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

INTEST supports internal chip testing.

When the TAP controller is in the state "update DR", all inputs are updated internally with the falling edge of TCK. When it has entered state "capture DR" the levels of all outputs are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

0001 (INTEST) is the default value of the instruction register.

SAMPLE/PRELOAD provides a snap-shot of the pin level during normal operation or is used to preload (TDI) / shift out (TDO) the boundary scan with a test vector. Both activities are transparent to the system functionality.

IDCODE Register

The 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to "1".

Version	Device Code	Manufacturer Code		Output
0001	0000 0000 0110 0111	0000 1000 001	1	--> TDO

Note: In the state "test logic reset" the code "0011" is loaded into the instruction code register.

CLAMP allows the state of the signals included in the boundary scan driven from the PEF 24901 to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. These output signals driven from the DFE-T V2.2 will not change while CLAMP is selected.

HIGHZ sets all output pins included to the boundary scan path into a high impedance state. In this state, an in-circuit test system may drive signals onto the connections

normally driven by the DFE-T V2.2 outputs without incurring the risk of damage to the DFE-T V2.2.

BYPASS, a bit entering TDI is shifted to TDO after one TCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

5 Monitor Commands

This chapter summarizes the Monitor commands and messages that are available for DFE-T V2.2. Please refer to section **Chapter 3.2.3** for a detailed description of the Monitor handshake procedure.

Defined MON-8 Commands for DFE-T V2.2

In **Table 19** the Monitor-8 commands are defined[1]. Each command is executed after having been transferred by proper use of the handshake procedure.

.

Table 19   Defined MON-8 Commands for DFE-T V2.2

Code (Hex)	D	U	Function
80 00	RID		Read Identification requests the U-Transceiver to issue the ID code
80 EF	RDS		Read and Reset the Block Error Counter
81 7X (X= DCBA)	SETD		Set Relay Driver Pins DiA, DiB, DiC, DiD per port the status of 4 output pins can be set via this MON-8 command, Binary: 1000 0001 0111 DCBA
81 00	RST		Read Request of Status Pins via this MON-8 command information on the current status of general purpose input pins can be retrieved, per port 2 status pins are provided

The indications are summarized in **Table 20**. The messages "Answer Identification", "Answer Block Error Counter Read Request" and "Answer 'RST' Request" are two-byte messages.

.

Table 20   Defined MON-8 Indications for DFE-T V2.2

Code (Hex)	D	U	Function
80 08		AID	Answer Identification The DFE-T V2.2 replies the ID code.

---

[1] The DFE-T V2.2 responds to $87xx_H$ in the data downstream Monitor channel with $87xx_H$ in the data upstream Monitor channel, but no further action is initiated.

Table 20   Defined MON-8 Indications for DFE-T V2.2 (cont'd)

80 XX		ARDS	Answer Block Error Counter Read Request 2nd monitor byte contains the 8-bit counter value 'XX'
81 0X (X= $00S_1S_0$)		AST	Answer 'RST' Request also issued without request on change of either STi0, STi1 pin, Binary: 1000 1000 0000 $00S_1S_0$

6 Register Description

In this section the complete register map is described that is provided with the new MON-12 protocol. For the protocol details please refer to **Chapter 3.2.4**.

The register address arrangement is given in **Figure 28**. The U-interface registers are provided per line port. By register LP_SEL it can be determined which U register bank and by that which line port number is addressed. LP_SEL adds an offset value to the current address. The offset value is latched as long as register LP_SEL is overwritten again.
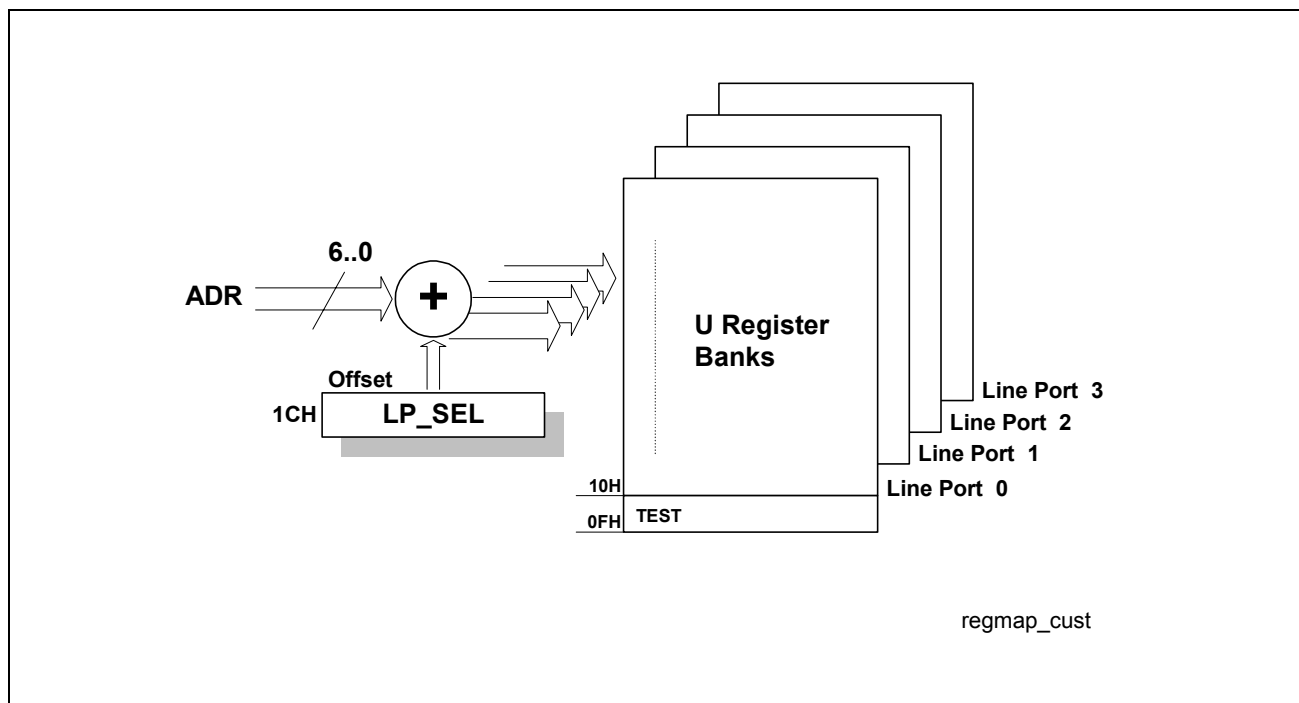

Figure 28 DFE-T V2.2 Register Map

6.1 Register Summary

	ADR	7	6	5	4	3	2	1	0	WR/ RD	1/n Ch.
TEST	$0F_H$	0	0	BER		0	0	0	0	**WR**/ RD*	1/4
LOOP	10_H	0	DLB	TRANS	U/ IOM	1	LBBD	LB2	LB1	**WR**/ RD*	1/4
RDS	12_H	Block Error Counter Value								RD	1/4
BERC	13_H	BERC Counter Value (Bit 15-8)								RD	1/4
	14_H	BERC Counter Value (Bit 7-0)									
LP_SEL	$1C_H$	0	0	0	0	0	0	LN2	LN1	**WR**/ RD*	1

*) read-back function for test use

Table 21   Register Map Reference Table

Reg Name	Access	Address	Reset Value	Comment	Page No.
TEST	WR	$0F_H$	00_H	**TEST Register** all test modes disabled	**93**
LOOP	WR	10_H	08_H	**LOOP Register** transparent loop mode set, all local loops deactivated	**94**
RDS	RD	12_H	00_H	**Running Digital Sum Counter**	**95**
BERC	RD	$13_H - 14_H$	0000_H	**BER Counter Value**	**96**
LP_SEL	WR	$1C_H$	00_H	**Line Port Selection Reg.** line port 1 is selected by default	**96**

6.1.1 Reset of U-Transceiver Functions During Deactivation or with CI Code RESET

The following U-transceiver registers are reset upon transition to state 'deactivating' or with software reset:

.

Table 22   Reset of U-Transceiver Functions During Deactivation or with CI Code RESET

Register	Reset to	Affected Bits/ Comment
TEST	00_H	
LOOP		only the bits LBBD, LB2 and LB1 are reset

6.1.2   Mode Register Evaluation Timing

Registers TEST and LOOP are evaluated and executed immediately.

6.2   Detailed Register Description

6.2.1   TEST - Test Register

The **Test** register sets the U-transceiver in the desired test mode. Note that the test modes 'Data Through' and 'Send Single Pulses' are activated via the C/I channel or by pin strapping.

TEST   read*)/**write**   Address: $0F_H$
Reset value: 00_H

7	6	5	4	3	2	1	0
0	0	BER		0	0	0	0

BER   Bit Error Rate Measurement Function

allows to measure the BER of the B1-, B2- and D-channel in the Transparent state,
prerequisite: closed loopback #2 on the NT side, reset of the BERC counter by read access and a continuous series of zeros is sent

00 =   Bit Error Rate (BERC) counter disabled

01 =   Reserved

10 =   Reserved

11 =   Bit Error Rate counter (BERC) is enabled,
starts BER measurement for the B1-, B2- and D-channel,
zeros are sent in channel B1, B2 and D

6.2.2 LOOP - Loopback Register

The **Loop** register controls local digital loopbacks of the DFE-T V2.2. The analog loopback (No. 1) and remote loopbacks are closed by use of C/I codes. For the loopback configurations that are available by the LOOP register see also **Chapter 4.4.1**.

LOOP   read*)/**write**   Address: 10_H
Reset value: 08_H

7	6	5	4	3	2	1	0
0	DLB	TRANS	U/IOM®	1	LBBD	LB2	LB1

DLB   Close Framer/Deframer loopback
the loopback is closed at the analog/digital interface
prerequisite is that LB1, LB2, LBBD and U/IOM® are set to '0'
only user data is looped and no maintenance data is not looped back
the DLB loop operates always in transparent mode

0 =   Framer/Deframer loopback open

1 =   Framer/Deframer loopback closed

TRANS   Transparent/ Non-Transparent Loopback
in transparent mode data is both passed on and looped back whereas in non-transparent mode data is not forwarded but substituted by '1's (idle code) and just looped back
if LBBD, LB2, LB1 is closed towards the IOM® interface and bit TRANS is set to '0' then the state machine has to be put into state 'Transparent' first (e.g. by C/I = DT) before data is output on the U-interface
bit TRANS has no effect on DLB (always transparent) and the analog loopbacks (AR1 operates always in transparent mode)

0 =   transparent mode

1 =   non-transparent mode
'1's are sent on the IOM®-2 interface in the corresponding time-slot

U/IOM®   Close LBBD, LB2, LB1 Towards U or Towards IOM®
Switch that selects whether loopback LB1, LB2 or LBBD is closed towards U or towards IOM®-2
the setting affects all test loops, LBBD, LB2 and LB1
an individual selection for LBBD, LB2, LB1 is not possible

       0 =   LB1, LB2, LBBD loops are closed from IOM®-2 to IOM®-2

       1 =   LB1, LB2, LBBD loops are closed from U to U

LBBD   Close complete loop (B1, B2, D) near the system interface
the direction towards the loop is closed is determined by bit 'U/IOM®'

       0 =   complete loopback open

       1 =   complete loopback closed

LB2   Close loop B2 near the system interface
the direction towards the loop is closed is determined by bit 'U/IOM®'

       0 =   loopback B2 open

       1 =   loopback B2 closed

LB1   Close loop B1 near the system interface
the direction towards the loop is closed is determined by bit 'U/IOM®'

       0 =   loopback B1 open

       1 =   loopback B1 closed

6.2.3 RDS - Block Error Counter Register

The Block Error Counter register 'RDS' monitors and counts code violations of the near-end and far-end side. The counter stops at 255 and does not overflow. If the register is read out the block error counter is automatically reset to '0'.

The register value can be requested either by the MON-8 command 'RDS' or can be directly addressed using the MON-12 protocol.

RDS   read   Address: 12_H
Reset value: 00_H

7	6	5	4	3	2	1	0
			Block Error Counter Value				
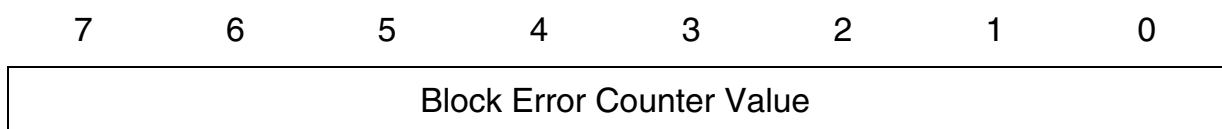
6.2.4 BERC - Bit Error Rate Counter Register

The **B**it **E**rror **R**ate **C**ounter register contains the number of bit errors that occurred during the period the bit TEST.BER was set active. If the low-significant register is read out the BERC register is automatically reset to '0'

BERC   read   Address: 13-14$_H$
Reset value: 0000$_H$

15	14	13	12	11	10	9	8
			Bit Error Rate Counter Value				

7	6	5	4	3	2	1	0
			Bit Error Rate Counter Value				
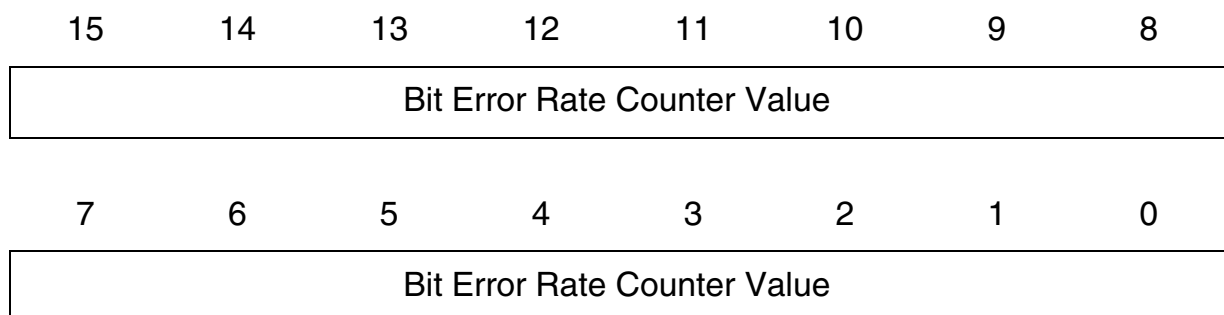
6.2.5 LP_SEL - Line Port Selection Register

The **Line Port Selection** register selects the register bank that is associated with the addressed line port. All line port specific register operations - line port specific registers are indicated by a '4' in the last column of the register summary - are performed on the line port that is addressed by the value of LP_SEL.

LP_SEL   read/**write**   Address: 1C$_H$
Reset value: 00$_H$

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LN2	LN1
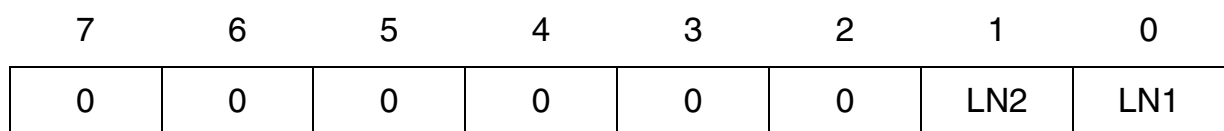
LN2,1   Line Port Number

    00 =   Line port no. 0 is addressed by the following command

    01 =   Line port no. 1 is addressed by the following command

    10 =   Line port no. 2 is addressed by the following command

    11 =   Line port no. 3 is addressed by the following command

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 125	°C
IC supply voltage	V_{DD}	– 0.3 to 4.6	V
Input/Output voltage on Input pins and on high ohmic Output pin with respect to ground	V_S	– 0.3 to 5.5	V
Maximum current supplied to any pin for more than 5 ms	I_{max}	10	mA
ESD robustness[1] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	2000	V

[1] According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	– 40	85	°C	
Supply voltage	V_{DD}	3.0	3.6	V	
Ground	V_{SS}	0	0	V	
Voltage applied to input pin	V_S	-0.3	V_{DD} + 3.3 (max. 5.25)	V	
Voltage applied to output pin in high-ohmic state (open drain)	V_S	-0.3	V_{DD} + 3.3 (max. 5.25)	V	

Note: In the operating range, the functions given in the circuit description are fulfilled.

7.3 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	**max.**		
Input low voltage	V_{IL}	– 0.3	0.8	V	
Input high voltage[1]	V_{IH}	2.0	5.25	V	
Output low voltage	V_{OL}		0.45	V	I_{OL} = 7 mA [2] I_{OL} = 2 mA [3]
Output high voltage	V_{OH}	2.4		V	I_{OH} = – 7 mA [1] I_{OH} = – 2 mA [2]
Input leakage current	I_{IL}	-1	1	µA	V_{DD} = 3.3 V, V_{SS} = 0 V; all other pins are floating; 0 V< V_{IN} < V_{DD}
Output leakage current	I_{OZ}	-1	1	µA	V_{DD} = 3.3 V, V_{SS} = 0 V; 0 V< V_{OUT} < V_{DD}
Input pull down current	I_{PD}	50	200	µA	V_{IN} = V_{DD}
Input pull up current	I_{PU}	-170	-50	µA	V_{IN} = V_{SS}

[1] Apply to all inputs and to DOUT in high ohmic state

[2] Apply to: DOUT

[3] Apply to all other Output pins except DOUT

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

7.4 AC Characteristics

Inputs are driven to 2.4 V for a logical '1' and to 0.45 V for a logical '0'. Timing measurements are made at 2.0 V for a logical '1' and 0.8 V for a logical '0'. The AC testing input/output waveforms are shown in **Figure 29.**

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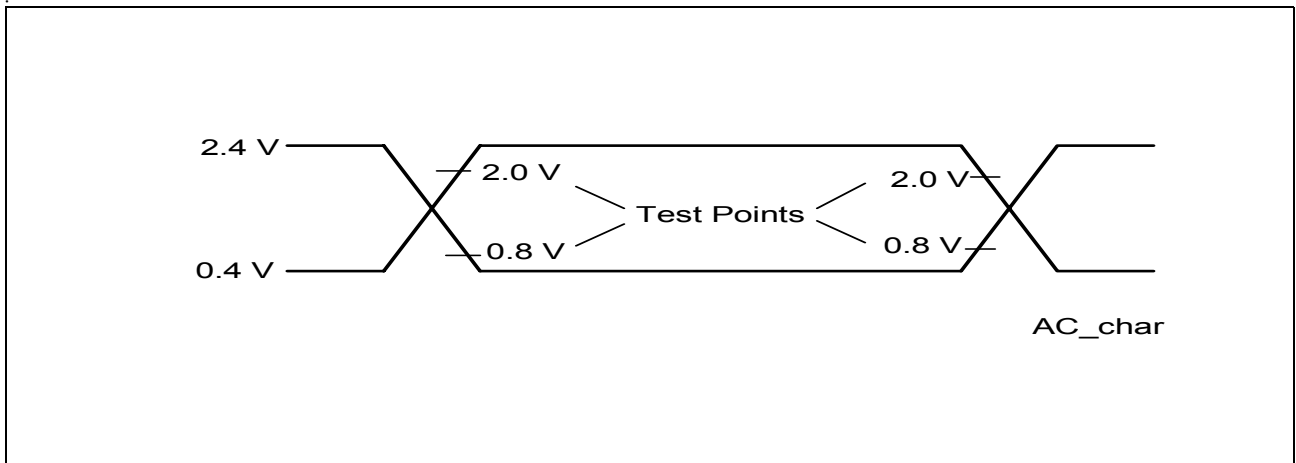
Figure 29   Input/Output Waveform for AC Tests

7.4.1 Reset Timing

.

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Active Low Period	$t_{\overline{RES}}$	200		ns	**the end of reset execution is delayed internally for 900 μs with respect to the low active phase** 15.36 MHz master clock has to be applied

.
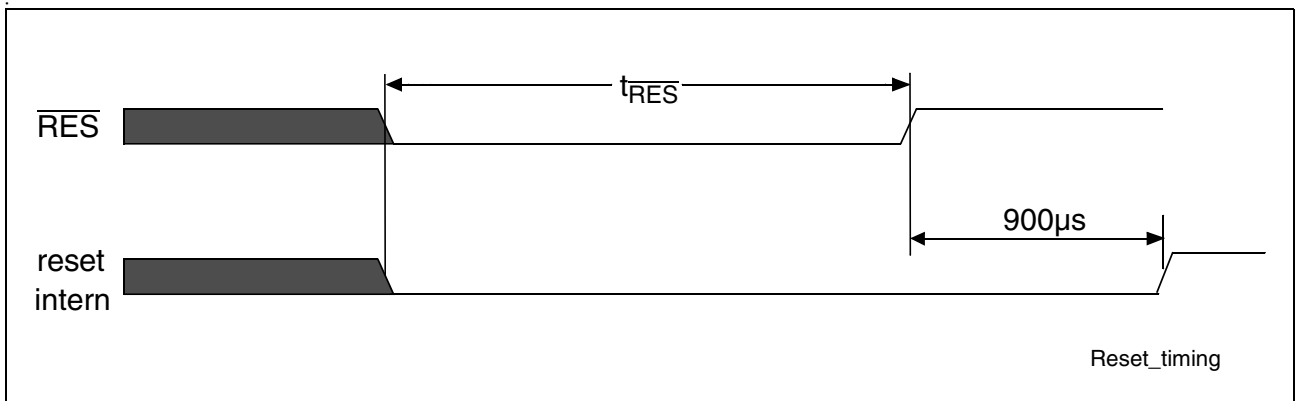
Figure 30   Reset Timing

7.4.2   IOM®-2 Interface Timing

The dynamic characteristics of the IOM®-2-interface are given in **Figure 31**. In case the period of signals is stated the time reference will be at 1.4 V; in all other cases 0.8 V (low) and 2.0 V (high) thresholds are used as reference.
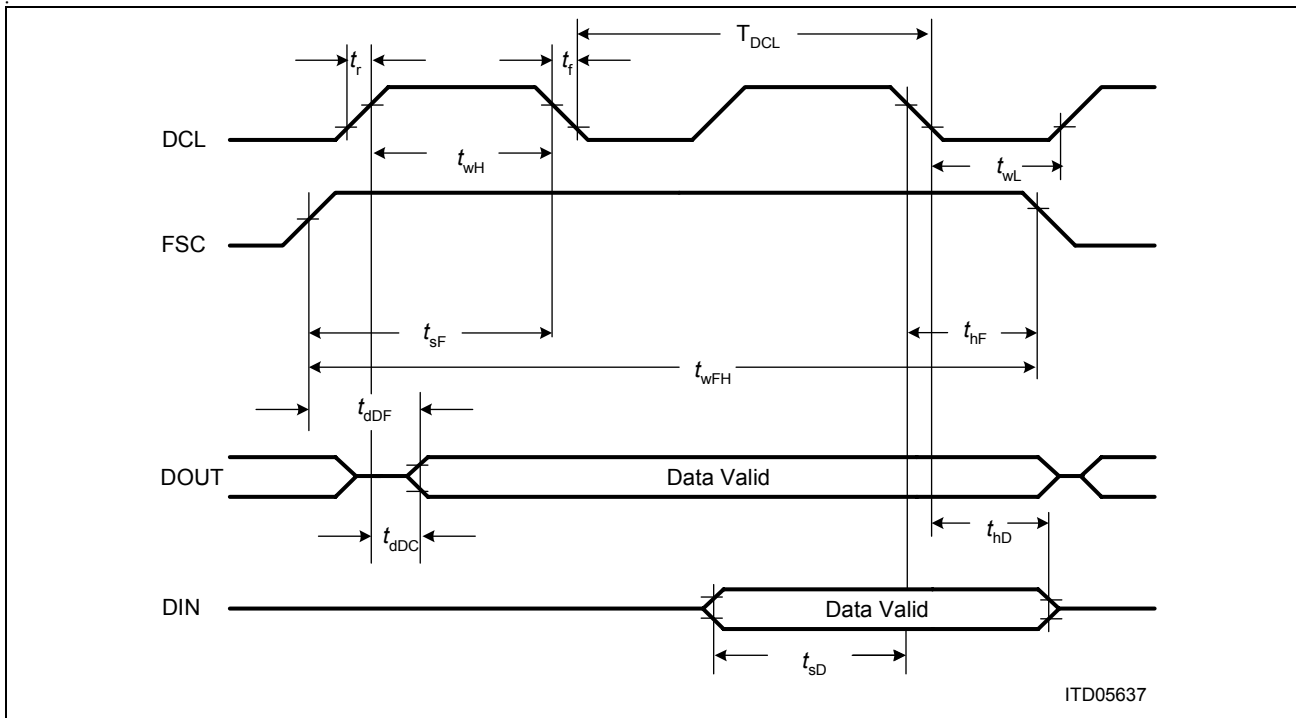
Figure 31   IOM®-2 Interface Timing (Double Clock Mode)

Table 23   IOM®-2 Dynamic Input Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DCL rise/fall time	t_r, t_f			60	ns
DCL period	T_{DCL}	122			ns
DCL pulse width, high low	t_{wH} t_{wL}	53 53	$(T_{DCL})/2$ $(T_{DCL})/2$		ns ns
FSC rise/fall	t_r, t_f			60	ns
FSC setup time	t_{sF}	10			ns
FSC hold time	t_{hF}	10			ns
FSC pulse width, high low	t_{wFH} t_{wFL}	$2 \times T_{DCL}$ $2 \times T_{DCL}$			ns
DIN setup time	t_{sD}	10			ns
DIN hold time	t_{hD}	10			ns

Table 24   IOM®-2 Dynamic Output Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
DCL Data delay clock [1] Pin PUP = '0'	t_{dDC}			100	ns	C_L = 150 pF, Charged with 5 V
Pin PUP = '1'	t_{dDC}			40	ns	C_L = 100 pF, Charged with 3.3 V
FSC Data delay frame [1]	t_{dDF}			20	ns	C_L = 150 pF

Notes: [1] The point of time at which the output data will be valid is referred to the rising edges of either FSC (t_{dDF}) or DCL (t_{dDC}). The rising edge of the signal appearing last (normally DCL) shall be the reference.

7.4.3   Interface to the Analog Front End

The AC characteristics of the AFE-interface pins are optimized to fit to AFE Version 2.1 if the following loads are not exceeded.

Table 25   Interface Signals of AFE and DFE-T

Pin	Signal Driving Device	Max. Capacitive Load Max. Connection Resistance
CL15	AFE	50 pF; 2 Ω
SDR	AFE	20 pF; 2 Ω
PDM0…3	AFE	20 pF; 2 Ω
SDX	DFE-T	20 pF; 2 Ω

7.4.4 Boundary Scan Timing
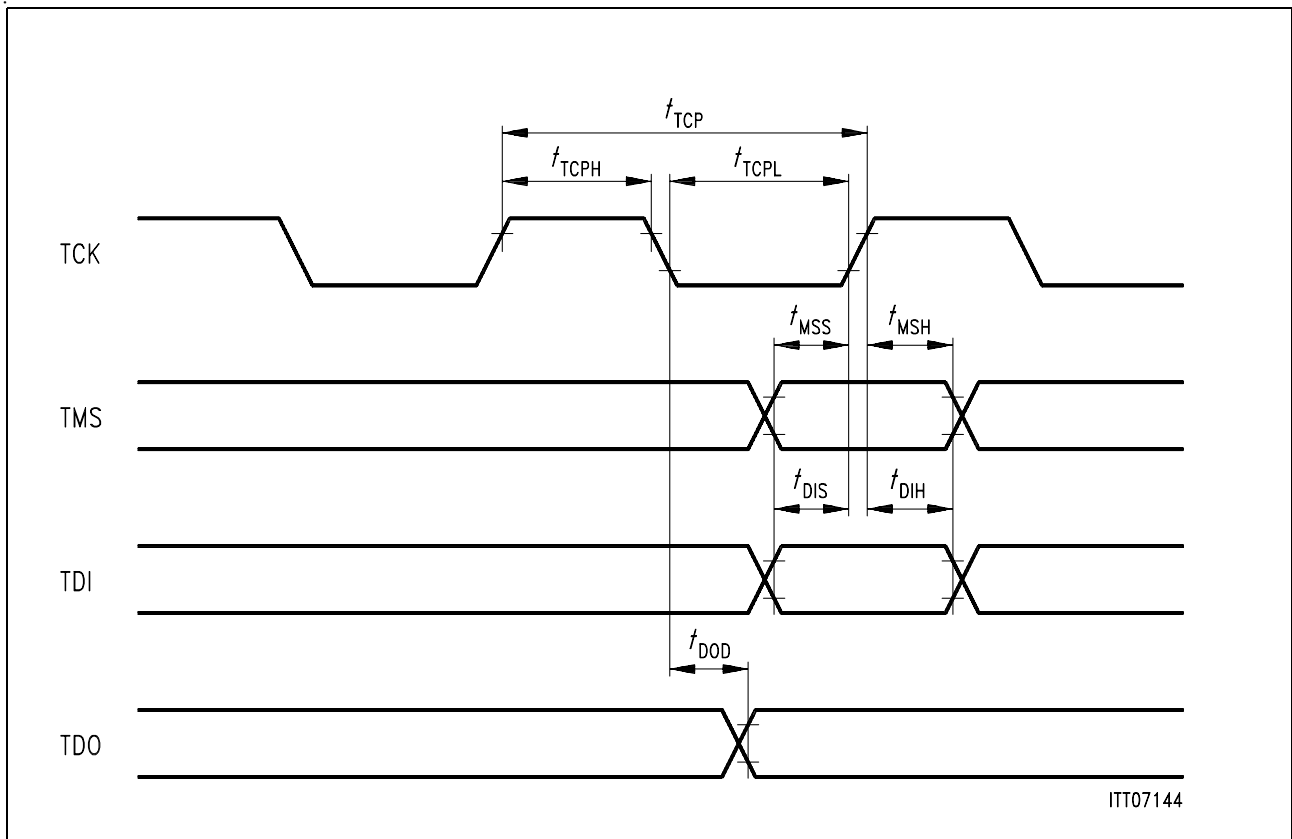
Figure 32   Boundary Scan Timing

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Table 26   Boundary Scan Dynamic Timing Requirements

Parameter	Symbol	Limit Values		Unit
		min.	max.	
test clock period	t_{TCP}	160	-	ns
test clock period low	t_{TCPL}	70	-	ns
test clock period high	t_{TCPH}	70	-	ns
TMS set-up time to TCK	t_{MSS}	30	-	ns
TMS hold time from TCK	t_{MSH}	30	-	ns
TDI set-up time to TCK	t_{DIS}	30	-	ns
TDI hold time from TCK	t_{DIH}	30	-	ns
TDO valid delay from TCK	t_{DOD}	-	60	ns

7.5 Capacitances

Parameter	Symbol	Limit Values		Unit	Notes
		min.	**max.**		
Input capacitance	C_{IN}		7	pF	
Output capacitance	C_{OUT}		10	pF	

7.6 Power Supply

7.6.1 Supply Voltage

V_{DD} to GND = +3.3 V ±0.3 V

7.6.2 Power Consumption

All measurements with random 2B+D data in active states, 3.3 V (0°C - 70°C)

Table 27   Power Consumption

Mode	Limit Values		Unit	Test Conditions
	typ.	**max.**		
Power-up all Channels	85	100	mA	3.3 V, open outputs, inputs at V_{DD} /V_{SS}
Power-down	33	35	mA	3.3 V, open outputs, inputs at V_{DD} /V_{SS}

8 Package Outlines

P-MQFP-64
(Plastic Metric Quad Flat Package)
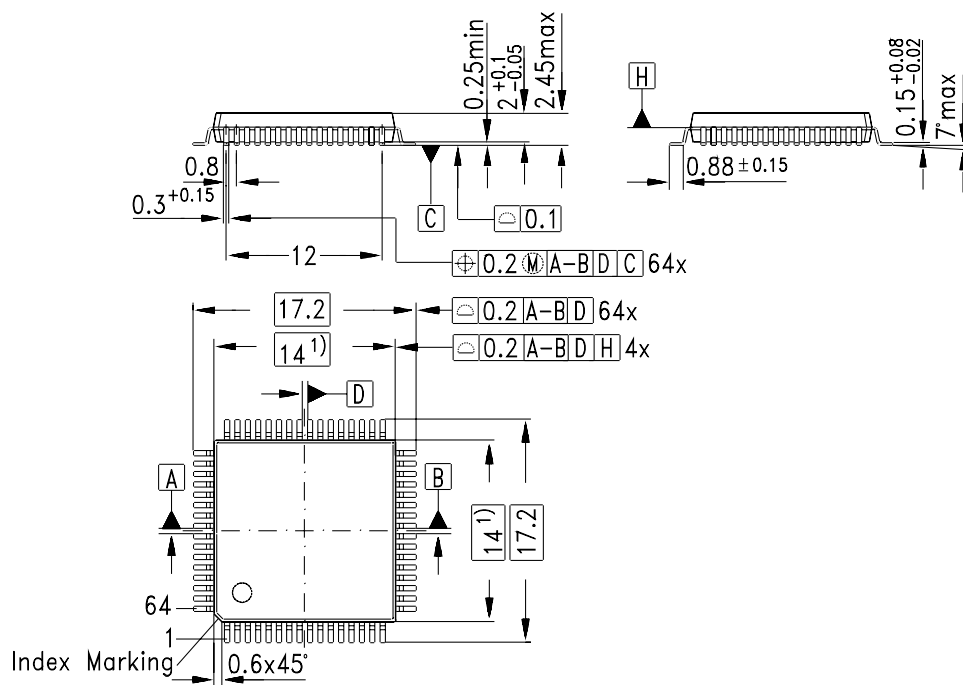
1) Does not include plastic or metal protrusions of 0.25 max per side

GPM05247

You can find all of our packages, sorts of packing and others in our
Infineon Internet Page "Products": http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

9   Appendix A: Standards and Specifications

The table below lists the relevant standards concerning transmission performance the DFE-T V2.2 claims to comply with.

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Organization		Valid for	Document	
ETSI	European Telecommunications Standards Institute	EU	TS 102 080 V1.3.1 (1998-11), formerly called ETR080	Transmission and Multiplexing (TM); Integrated Services Digital Network (ISDN) basic rate access; Digital transmission system on metallic local lines
FTZ	Fernmeledetechnisches Zentralamt	D	1 TR 220 08/91	Spezifikation der ISDN-Schnittstelle U_{k0} Schicht 1
			1 TR 210 11/87	ISDN Aktivierung/ Deaktivierung des Basisanschlusses Schicht 1
			1 TR 215 04/90	Euro-ISDN Aktivierung/ Deaktivierung des Basisanschlusses Schicht 1

10   Terminology

A

A/D	Analog to digital
ADC	Analog to digital converter
AGC	Automatic gain control
AIN	Differential U-interface input
ANSI	American National Standardization Institute
AOUT	Differential U-interface output

B

B1, B2	64-kbit/s voice and data transmission channel
BIN	Differential U-interface input
BOUT	Differential U-interface output

C

C/I	Command/Indicate (channel)

D

D	16-kbit/s data and control transmission channel
D/A	Digital-to-analog
DAC	Digital-to-analog converter
DCL	Data clock
DD	Data downstream
DT	Data through test mode
DU	Data upstream

E

EC	Echo canceller
EOM	End of message
ETSI	European Telephone Standards Institute

F

FEBE	Far-end block error
FIFO	First-in first-out (memory)
FSC	Frame synchronizing clock

G

GND	Ground

H

HDLC	High-level data link control

I

IEC-Q	ISDN-echo cancellation circuit conforming to 2B1Q-transmission code
IOM$^{®}$-2	ISDN-oriented modular 2nd generation
INFO	U- and S-interface signal as specified by ANSI/ ETSI
ISDN	Integrated services digital network

L

LBBD	Loop-back of B- and D-channels
LT	Line termination

M

MON	Monitor channel command
MR	Monitor read bit
MTO	Monitor procedure time-out
MX	Monitor transmit bit

N

NEBE	Near-end block error
NT	Network termination

P

PLL	Phase locked loop
PSD	Power spectral density
PTT	Post, telephone, and telegraph administration
PU	Power-up

R

RMS	Root mean square

S

S/T	Two-wire pair interface
SSP	Send single pulses (test mode)

T

TE	Terminal equipment

U

| U | Single wire pair interface |
| 4B3T | Transmission code requiring 120 kHz bandwidth |

11 Index

R

S

T

U

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"Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
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Dr. Ulrich Schumacher